VSC-HVDC

Protection

Requirements

6th HVDC Colloquium – DTU, Roskilde - Denmark

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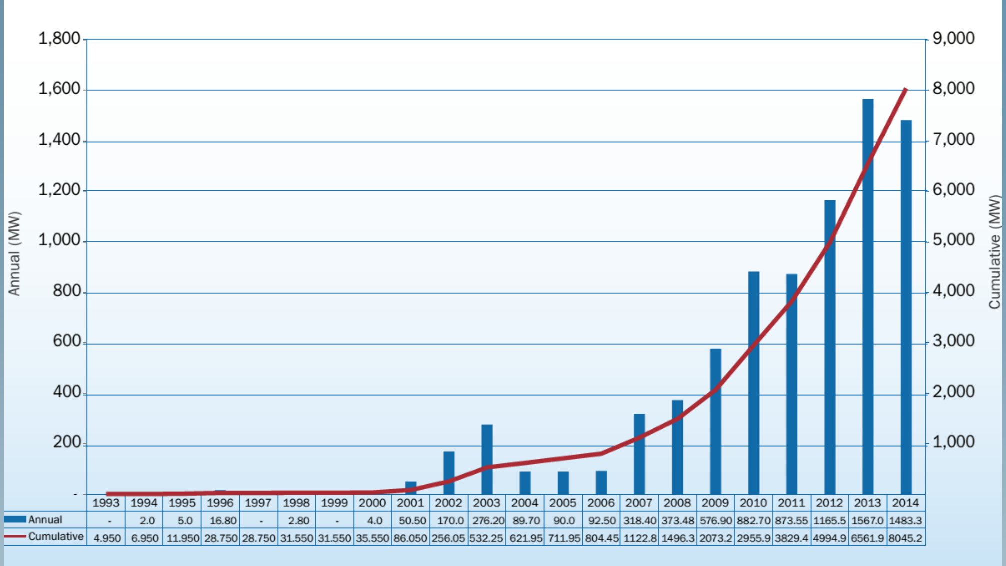
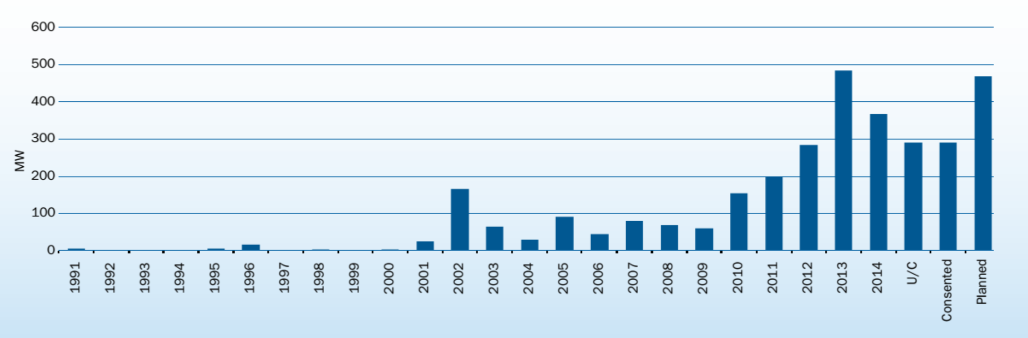
Offshore Wind Industry



	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014
Annual	-	2.0	5.0	16.80	-	2.80	-	4.0	50.50	170.0	276.20	89.70	90.0	92.50	318.40	373.48	576.90	882.70	873.55	1165.5	1567.0	1483.3
Cumulative	4.950	6.950	11.950	28.750	28.750	31.550	31.550	35.550	86.050	256.05	532.25	621.95	711.95	804.45	1122.8	1496.3	2073.2	2955.9	3829.4	4994.9	6561.9	8045.2



Installed Capacity and Average Wind Farm Size

418
new offshore wind turbines
in **12 wind farms**

34% MORE
than in 2012

2,080
turbines are installed
and grid connected

4 MW
average size offshore
wind turbines

work carried out in: **21** wind farms

new projects:
22 GW
of consented
wind farms

Source:EWEA

Offshore Wind Industry

Onshore wind sites are almost rare
Onshore wind sites are in northern parts
Solar sites are in the southern parts

Generation moves to borders

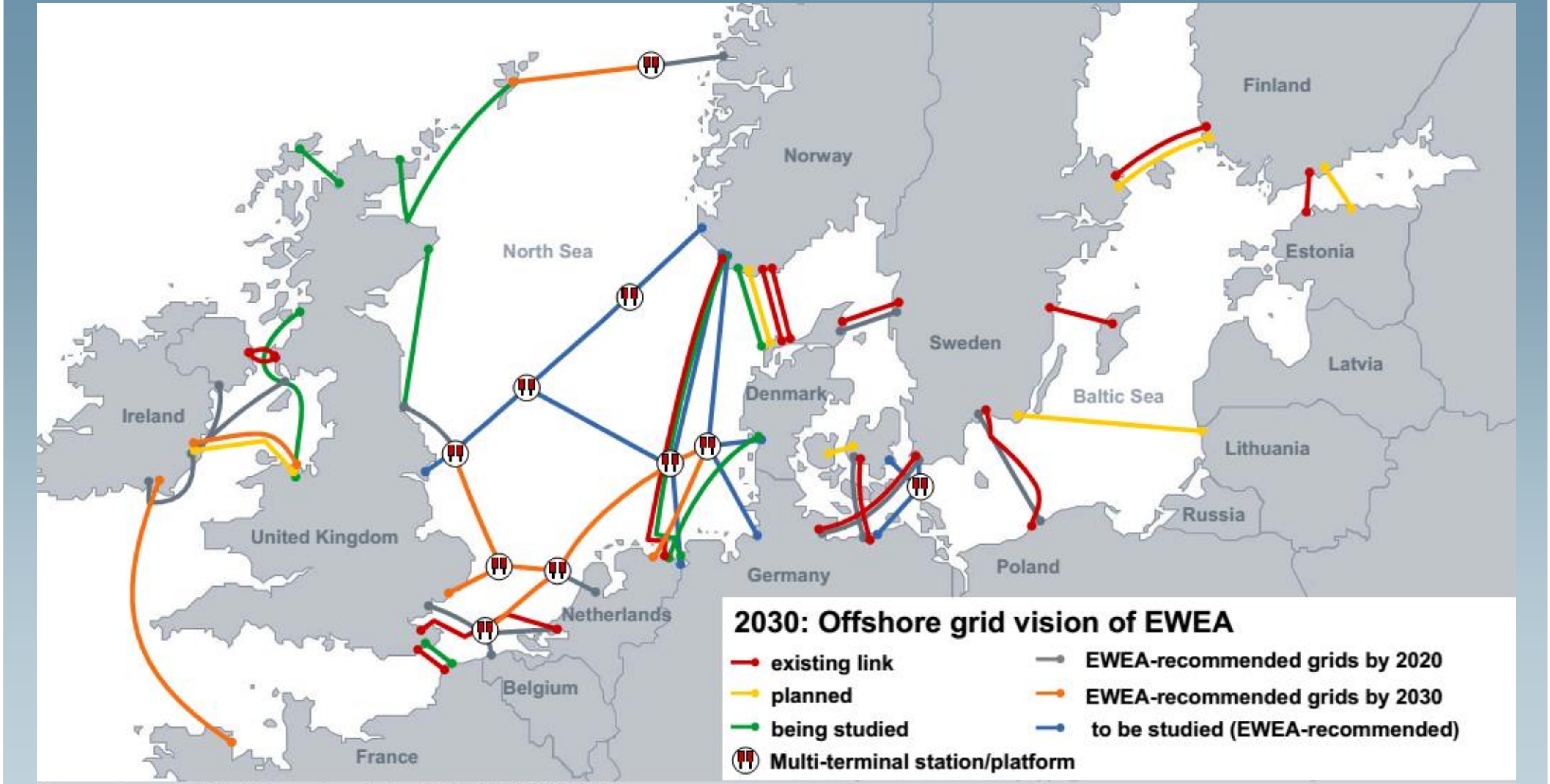
Population is far from generation

Demand for transmitting bulk amount of the energy over long distances

Point to point transmission lines
Multi-terminal and meshed grid

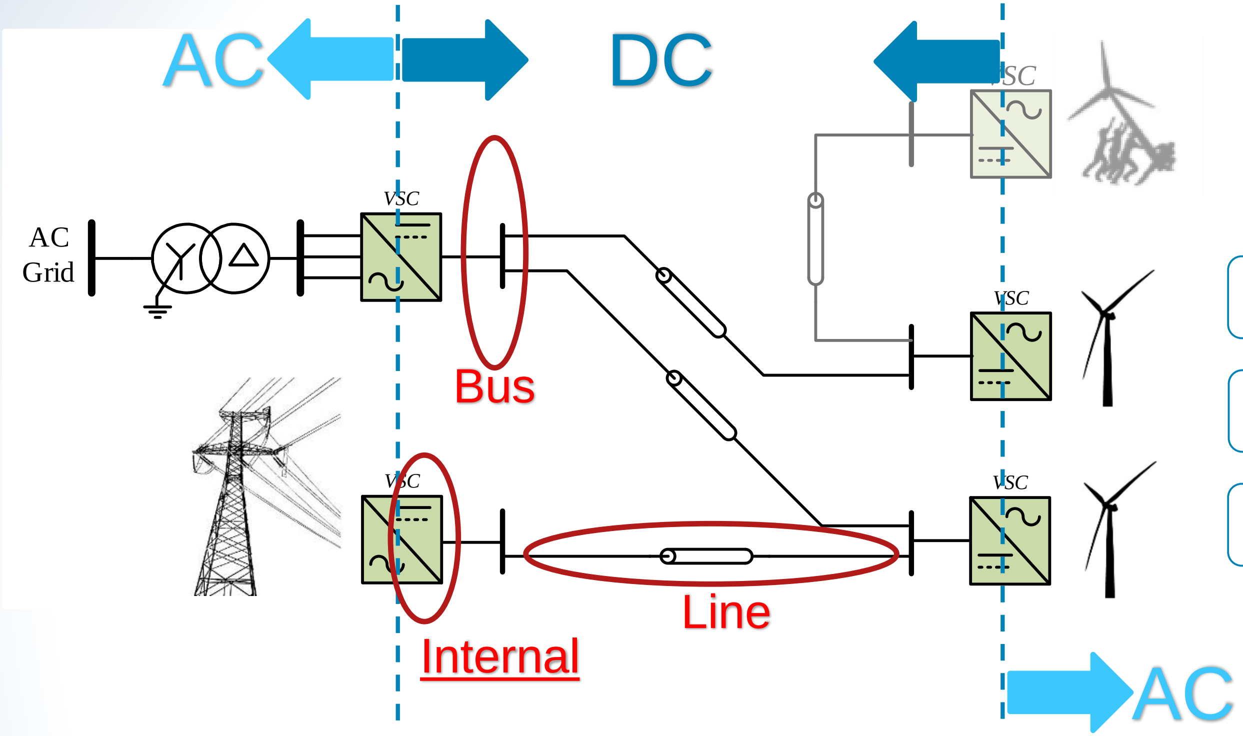
EWEA Target
2030
Offshore:
150GW
Onshore:
250GW

Multi-Terminal HVDC Grid



Source: European Wind Energy Association (EWEA) 2009/2010, Siemens

Multi-Terminal HVDC Grid



Protective Issues:

AC Side:

- Loss of Synchronism
- Frequency Deviation
- Symmetric Faults
- Asymmetric Faults

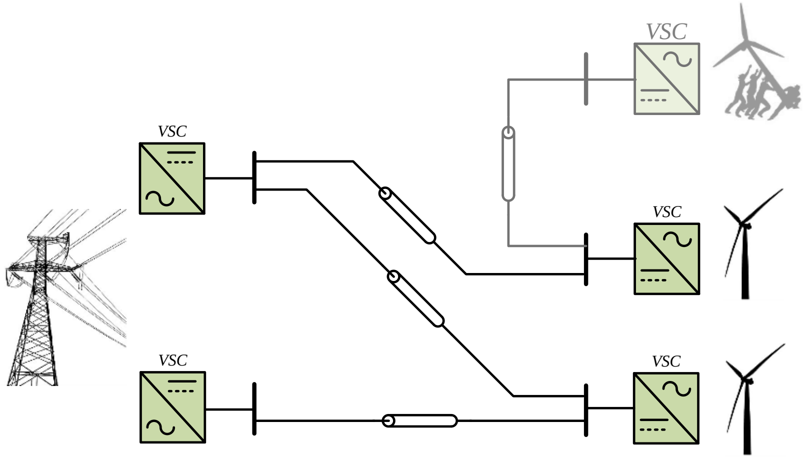
DC Side:

HVDC Line Faults:
Pole to Ground
Pole to Pole

DC Bus Faults:
Pole to Ground
Pole to Pole

Component Level:
Capacitors, Switches, Diodes, …

Multi-Terminal HVDC Grid



AC Side Faults Can be Handled because of full control on VSC at AC side fault.

Handling DC side faults is challenging!

Converter Main Circuit Topology

DC Link Capacitors Voltage Limitation

DC Line Parameters

DC Grid Stability Issues

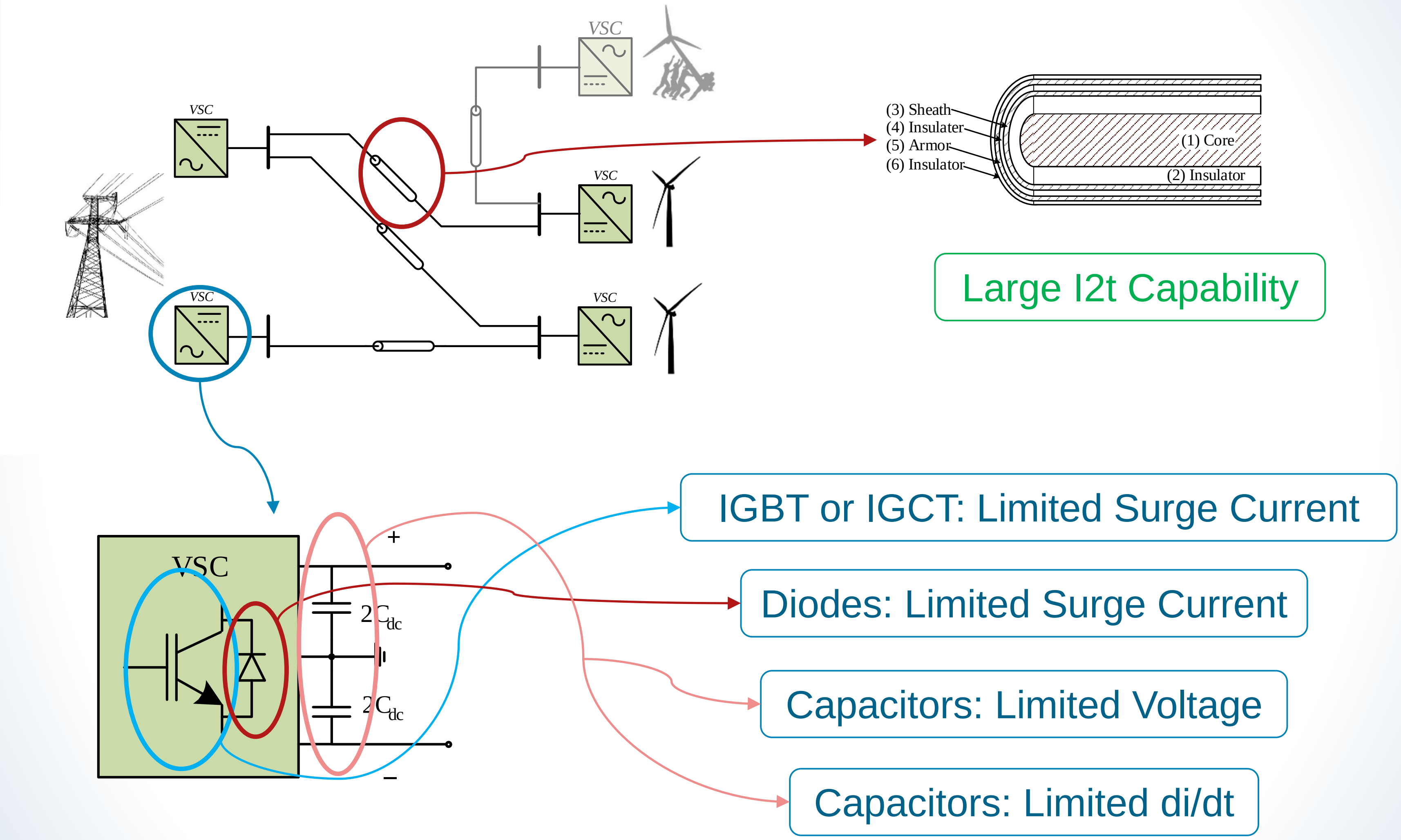
Diodes Overload Capability

Bypass Circuit Capability

IGBTs Surge Capability

Fault Current Contribution

What do we want to save!?



Large I2t Capability

IGBT or IGCT: Limited Surge Current

Diodes: Limited Surge Current

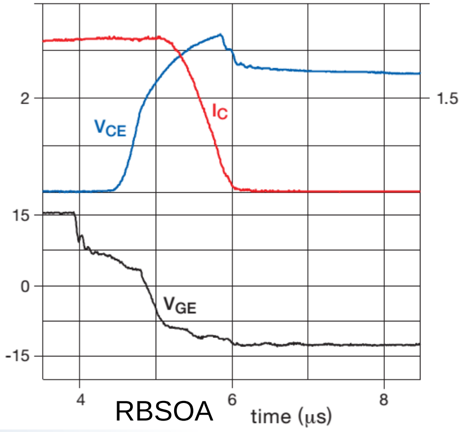
Capacitors: Limited Voltage

Capacitors: Limited di/dt

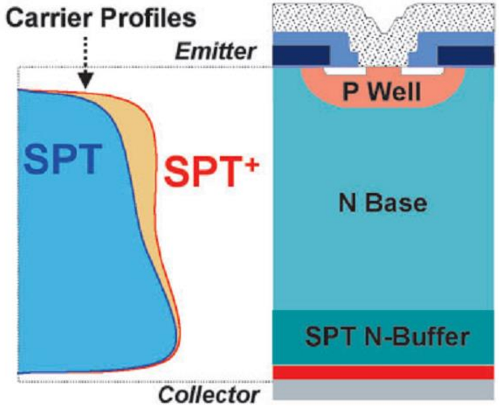
Power IGBTs

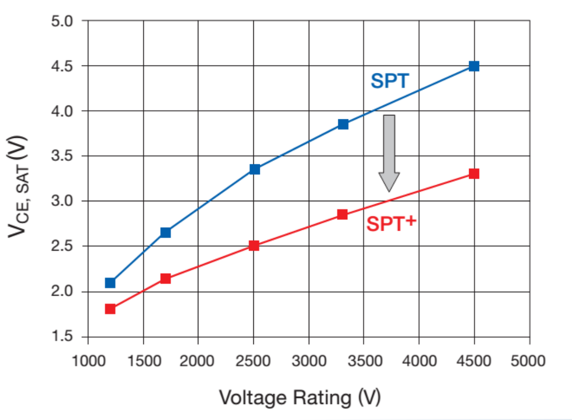
HiPak IGBT

- 3 Standard Isolation Voltages (4, 6 and 10.2kVRMS)
- AlSiC Base-plate (Good thermal cycling capability)
- AlN isolation (Low thermal resistance)
- Realized by Soft Punch Through Chip Technology
- Low Forward Voltage Drop Then Low Losses
- Soft Switching behavior, Large Safe Operation Area



RBSOA





Power IGBTs

StakPak IGBT

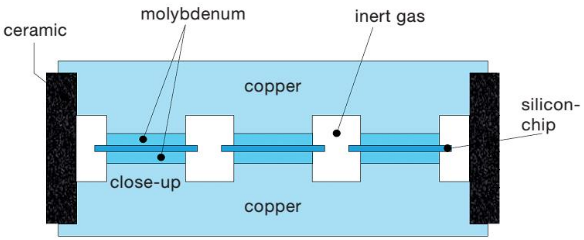
Optimized for Series Connections: Mechanically & Electrically

Stable Short-circuit Failure Mode (SCFM)

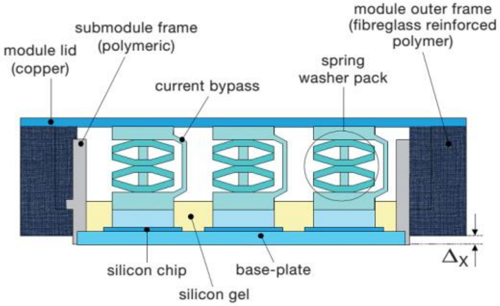
Reduced Flatness of Heat Sink Tolerance

Reduced Pressure Uniformity Requirement

Multi-level Converters with 6 or More Devices Mechanically in series



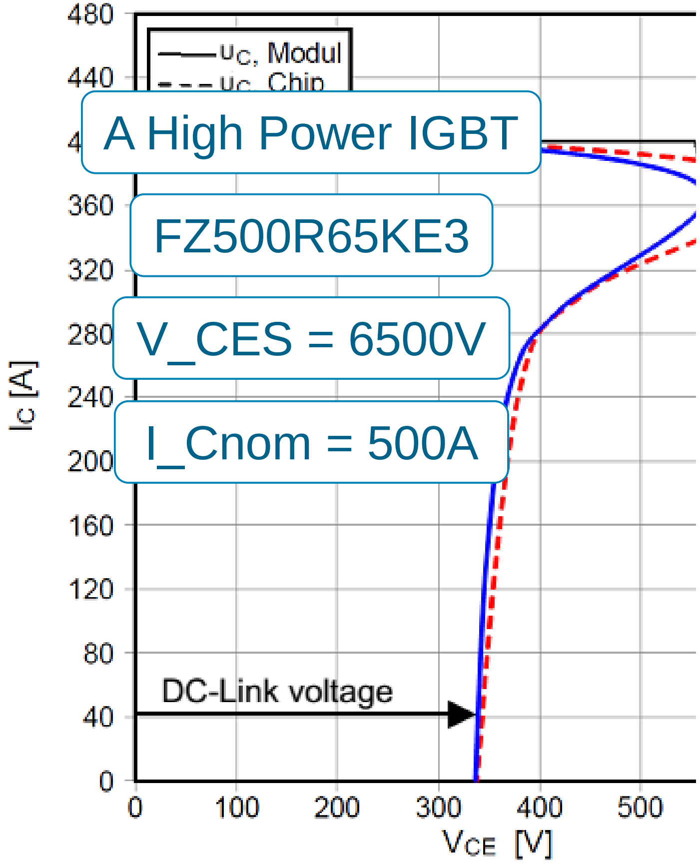
Chips contacted by common pole-piece



Chips contacted by individual springs

Power IGBTs

RBSOA



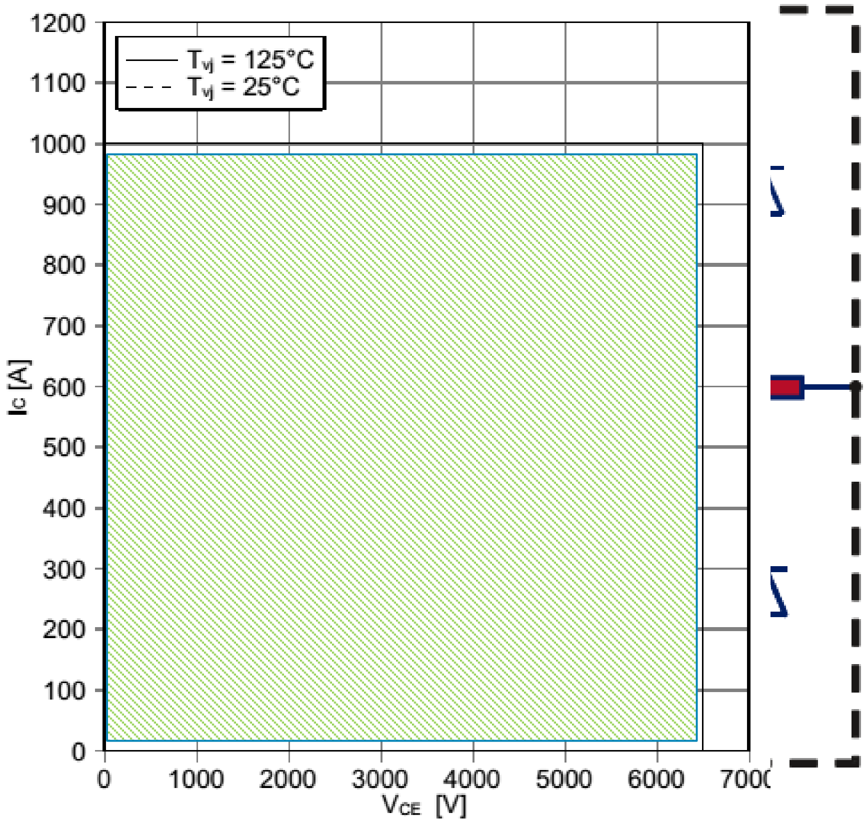
A High Power IGBT

FZ500R65KE3

V_CES = 6500V

I_Cnom = 500A

反偏安全工作区 IGBT, 逆变器 （RBSOA）
reverse bias safe operating area IGBT,Inverter (RBSOA)
$I_C = f(V_{CE})$
$V_{GE} = \pm 15$ V, $R_{Goff} = 10\ \Omega$, $T_{vj} = 125°C$



Power IGBTs

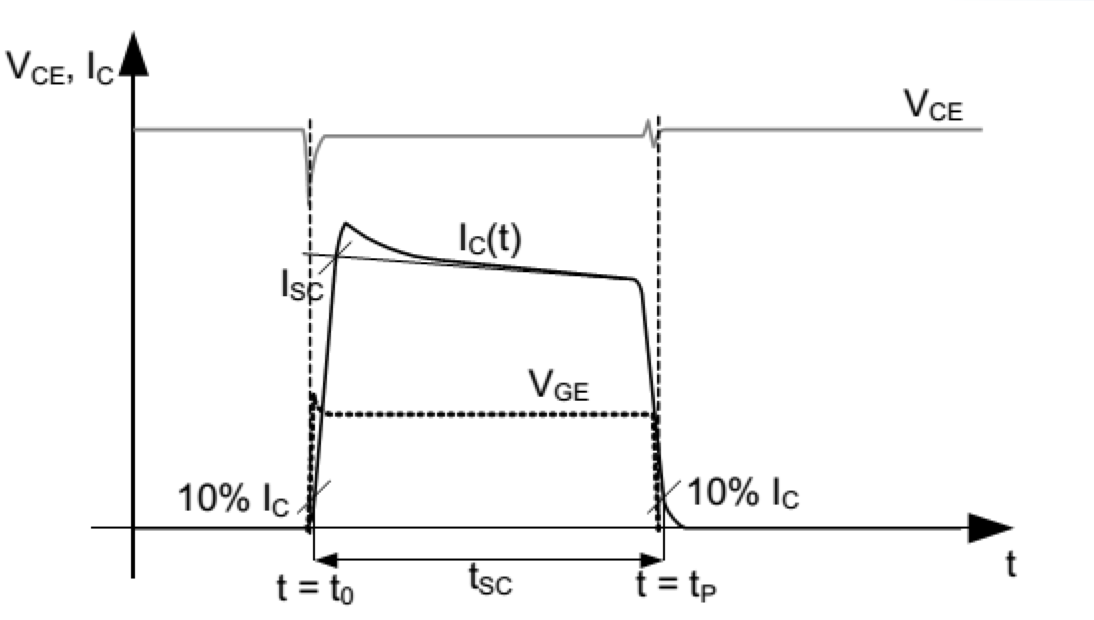
SCSOA

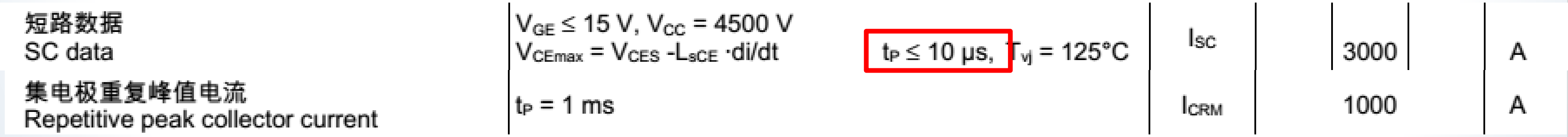
A High Power IGBT

FZ500R65KE3

V_CES = 6500V

I_Cnom = 500A





短路数据 SC data	$V_{GE} \le 15$ V, V_{CC} = 4500 V $V_{CEmax} = V_{CES} - L_{sCE} \cdot di/dt$	$t_P \le 10$ µs, T_{vj} = 125°C	I_{SC}		3000		A
集电极重复峰值电流 Repetitive peak collector current	t_P = 1 ms		I_{CRM}		1000		A

Diode SOA

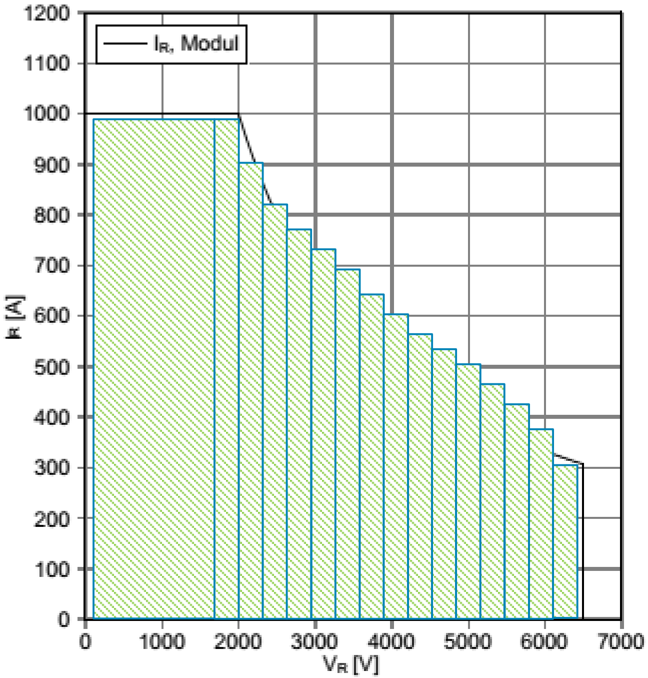
A High Power IGBT

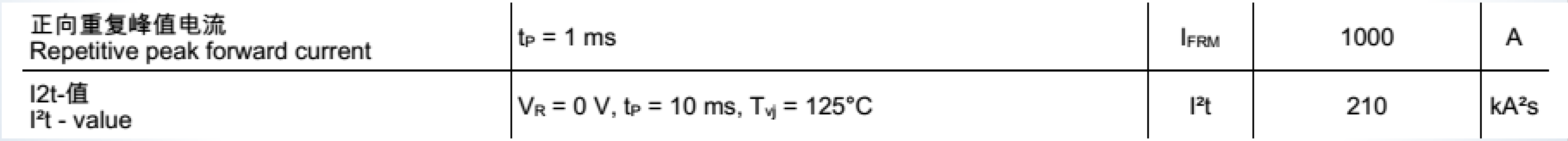
FZ500R65KE3

V_CES = 6500V

I_Cnom = 500A

安全工作区 二极管,逆变器 (SOA)
safe operation area Diode, Inverter (SOA)
$I_R = f(V_R)$
$T_{vj} = 125°C$





正向重复峰值电流 Repetitive peak forward current	t_P = 1 ms	I_{FRM}	1000	A
I2t-值 I^2t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C	I^2t	210	kA^2s

Topologies

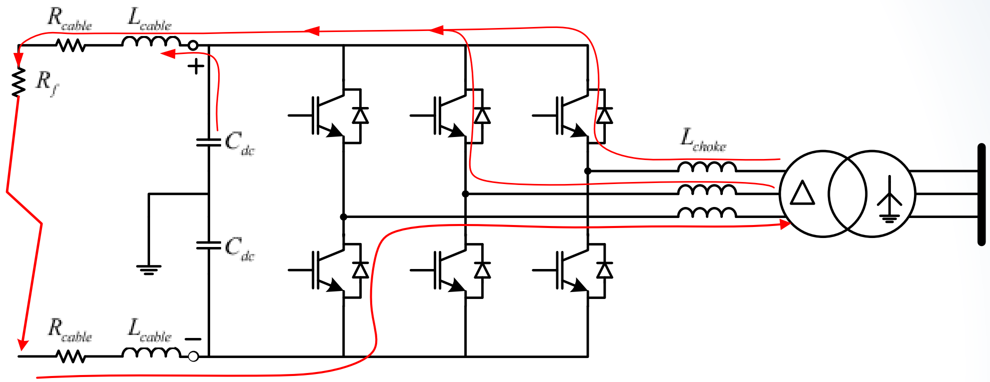
Two-level

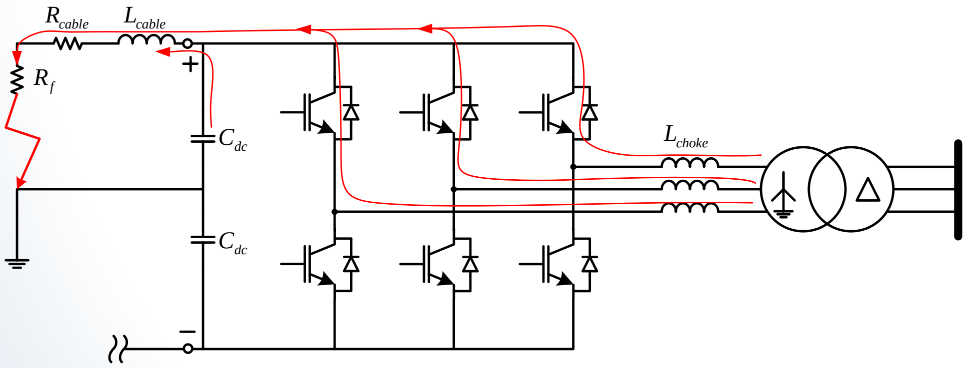
Pole to Pole Fault

Large Capacitor Contribution

AC Grid Contribution

Anti-parallel Diodes Stressed





Pole to Ground Fault

Capacitor Contribution

AC Grid Contribution

Anti-parallel Diodes Stressed

Topologies

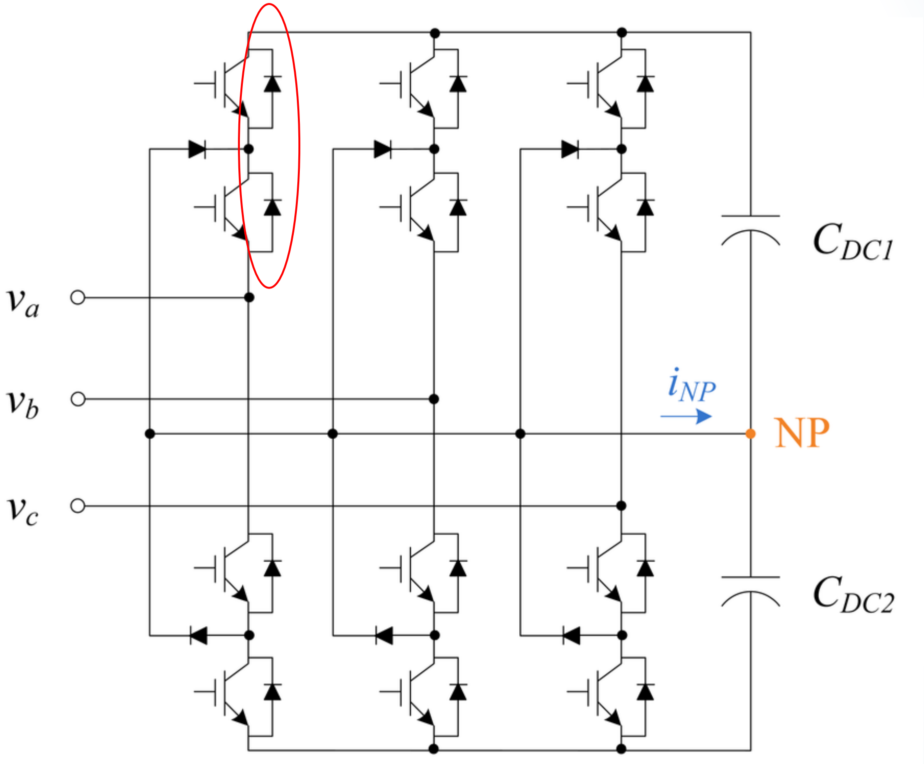
NPC & ANPC

Pole to Pole Fault

Large Capacitor Contribution

AC Grid Contribution

Anti-parallel Diodes Stressed

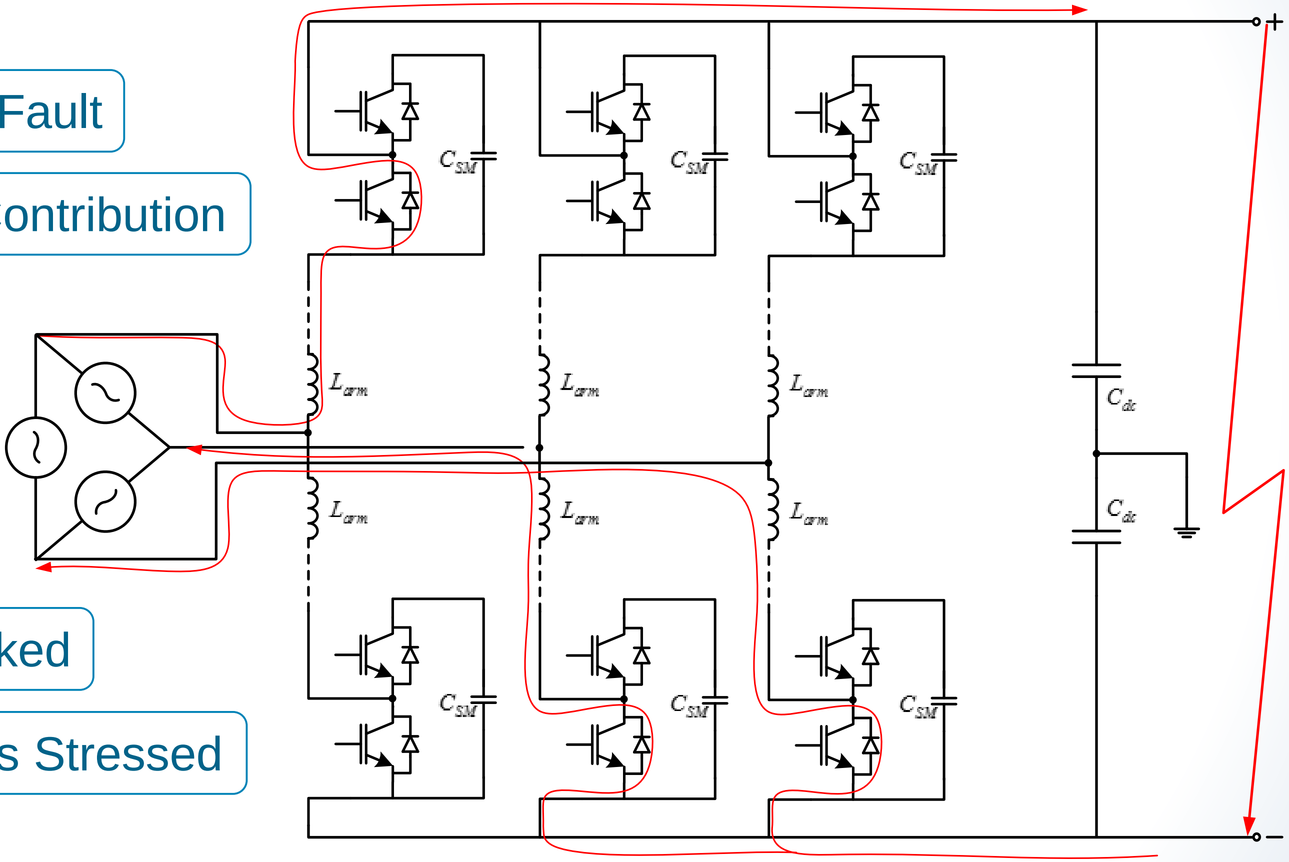


Topologies

H-Bridge MMC

Pole to Pole Fault

Partial Capacitor Contribution

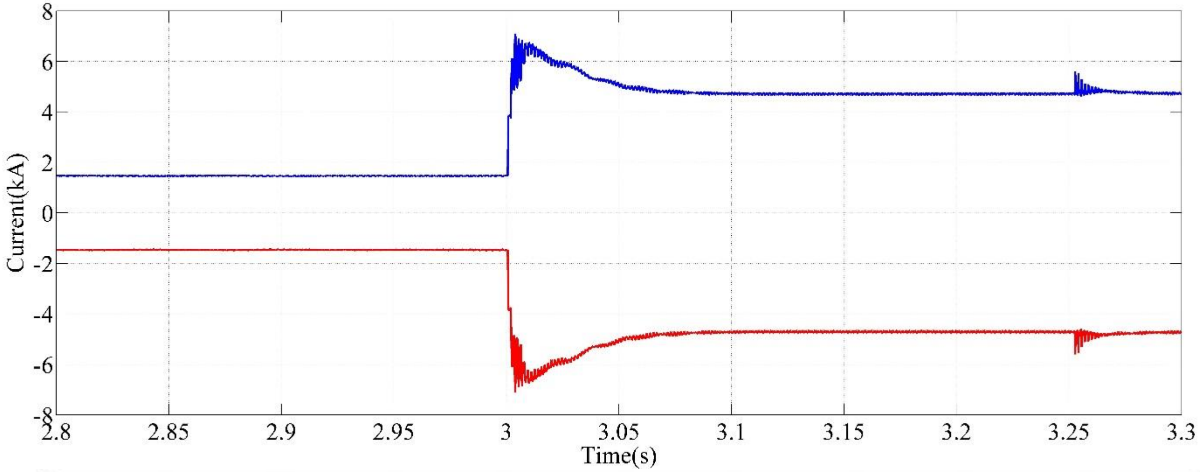


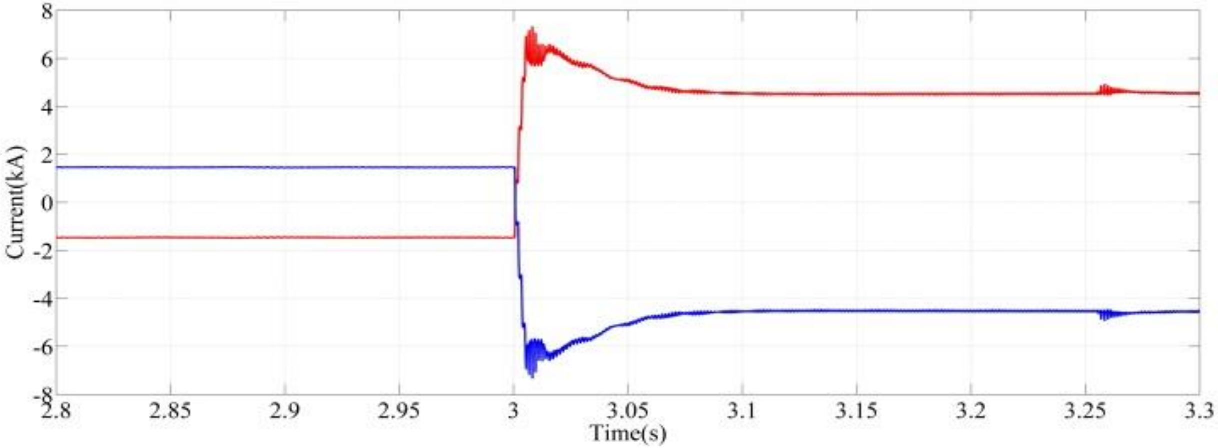
IGBTs Blocked

Anti-parallel Diodes Stressed

Topologies

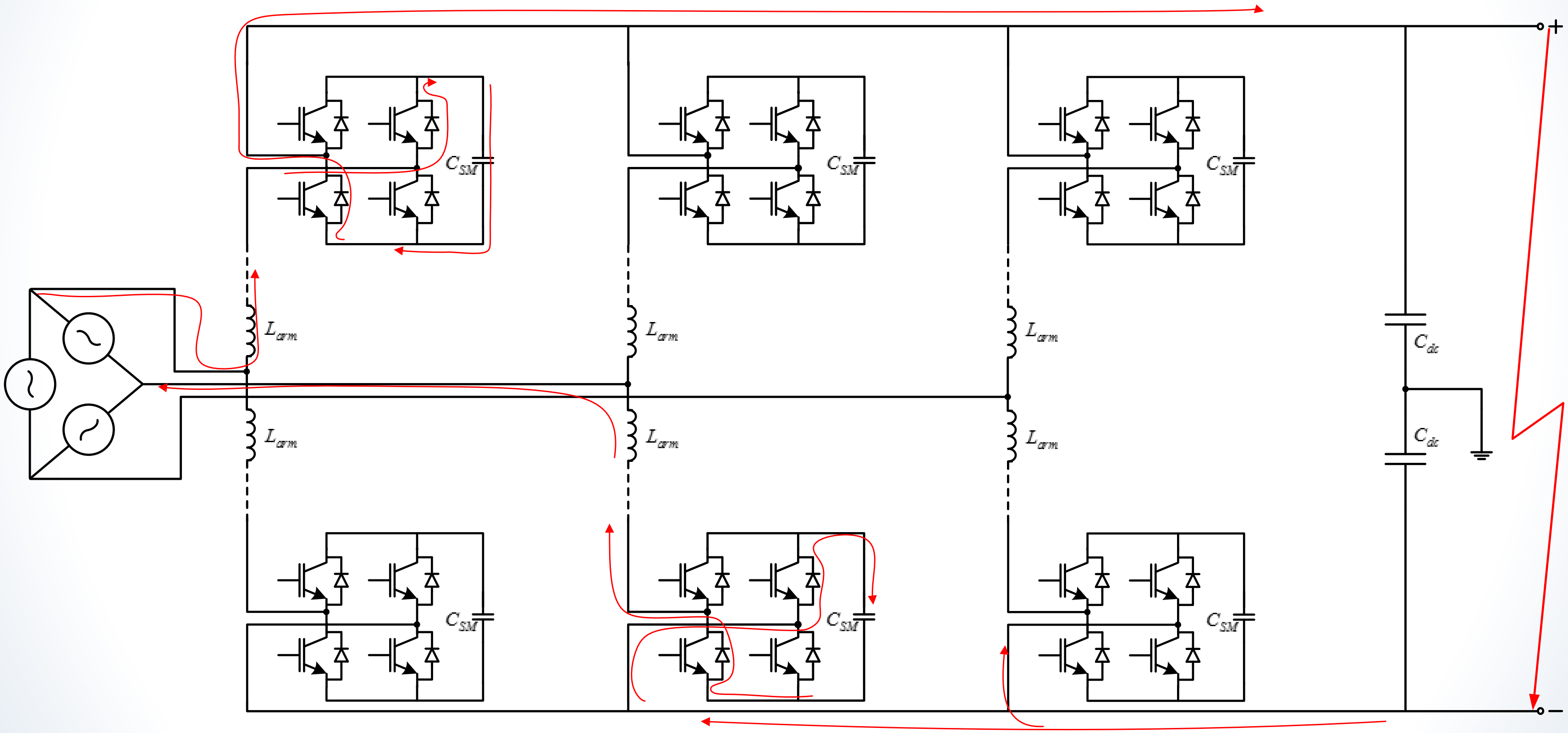
H-Bridge MMC





Topologies

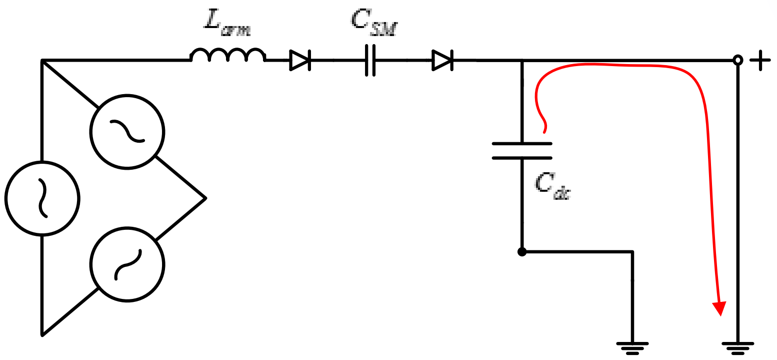
F-Bridge MMC

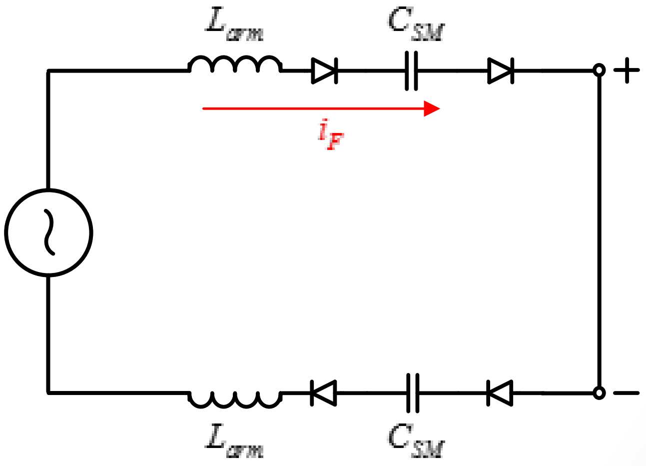


Topologies

F-Bridge MMC

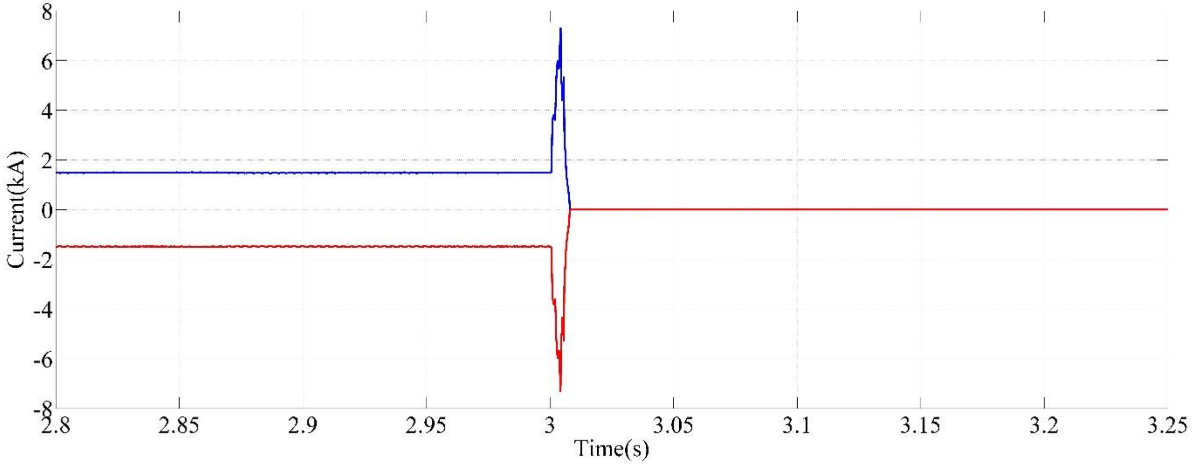
- Pole to Pole Fault
- Possible Capacitor Contribution
- IGBTs Blocked
- SM Capacitor Charged up
- DC Fault Blocked
- IGBTs Stressed Before Blocking

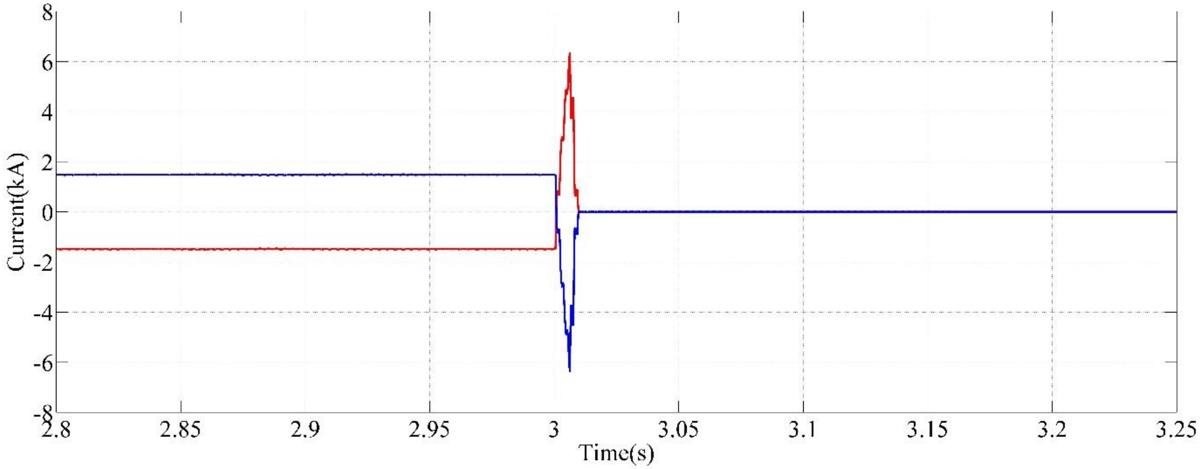




Topologies

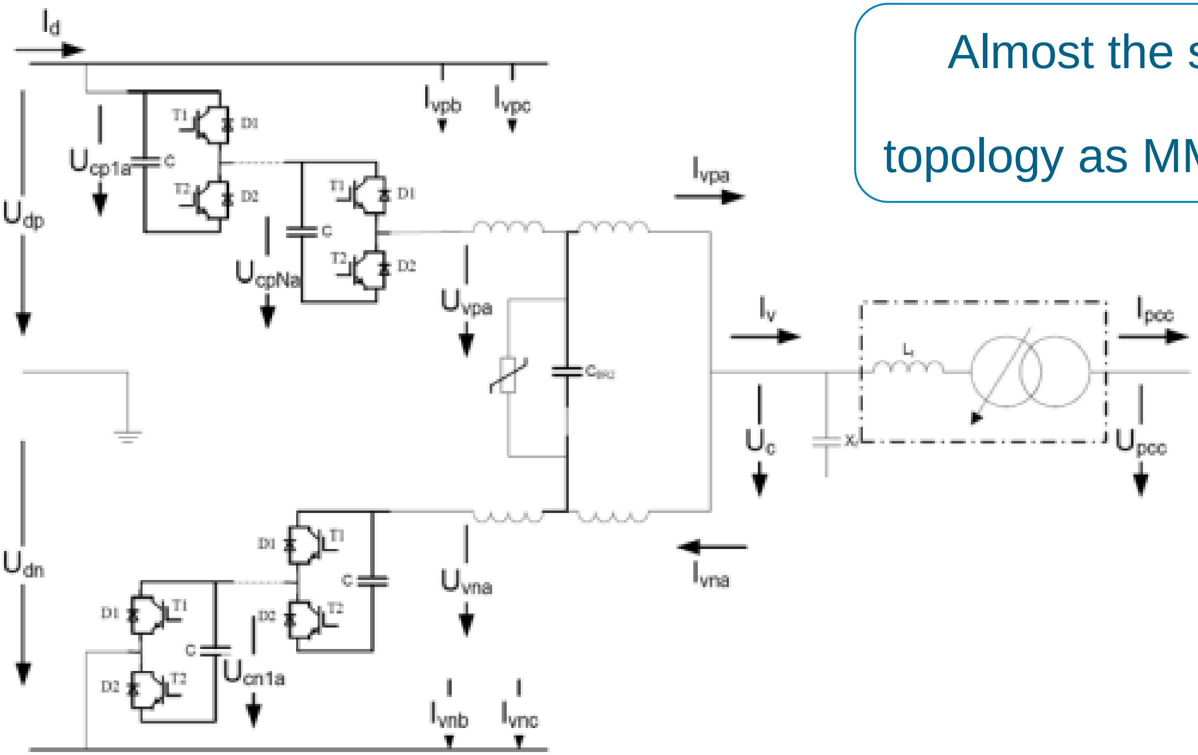
F-Bridge MMC





Topologies

ABB



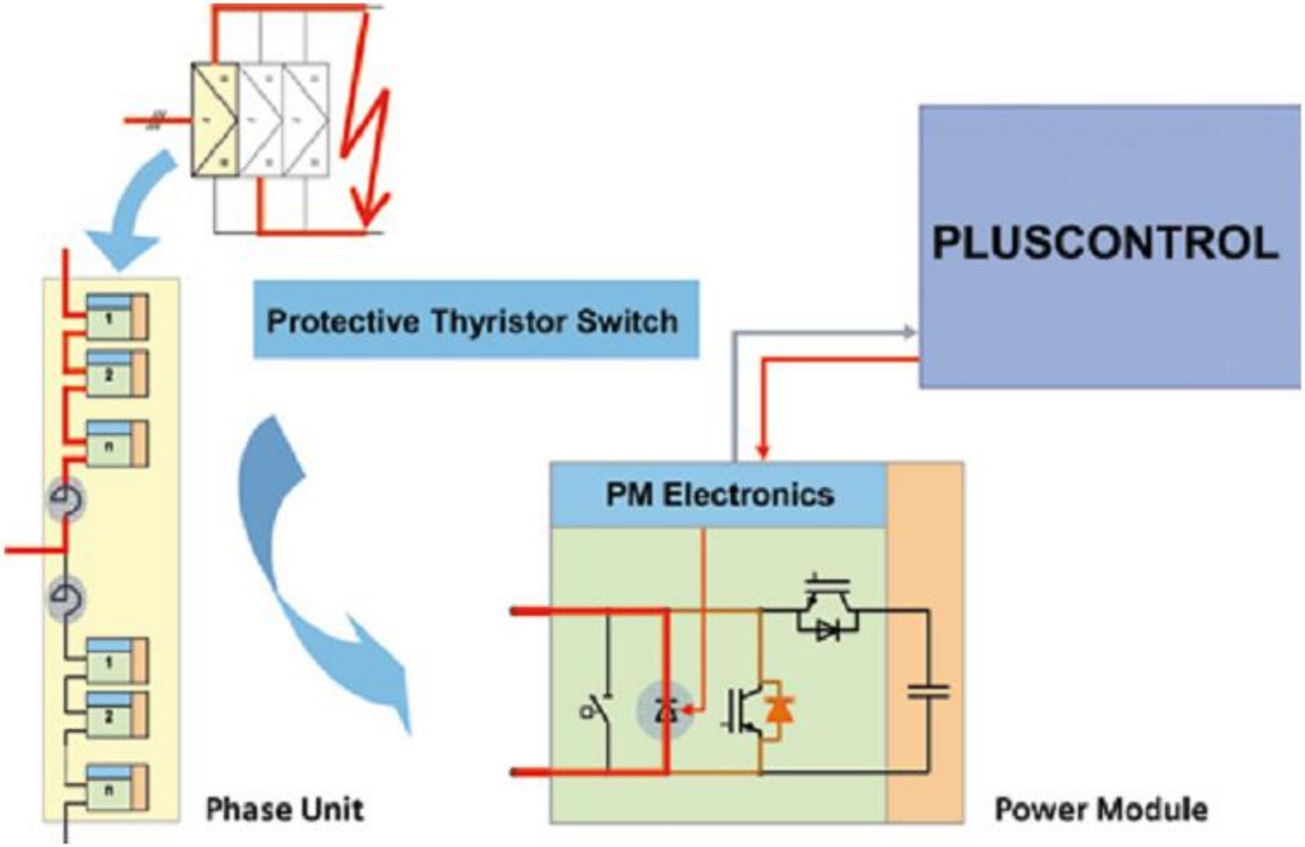
Jacobsson, B., Karlsson, P., Asplund, G., Harnefors, L., Jonsson, T., VSC - HVDC transmission with cascaded two-level converters, CIGRÉ session, Paris, 2010, paper reference B4-110.

Almost the same circuit

topology as MMC but redrawn

Topologies

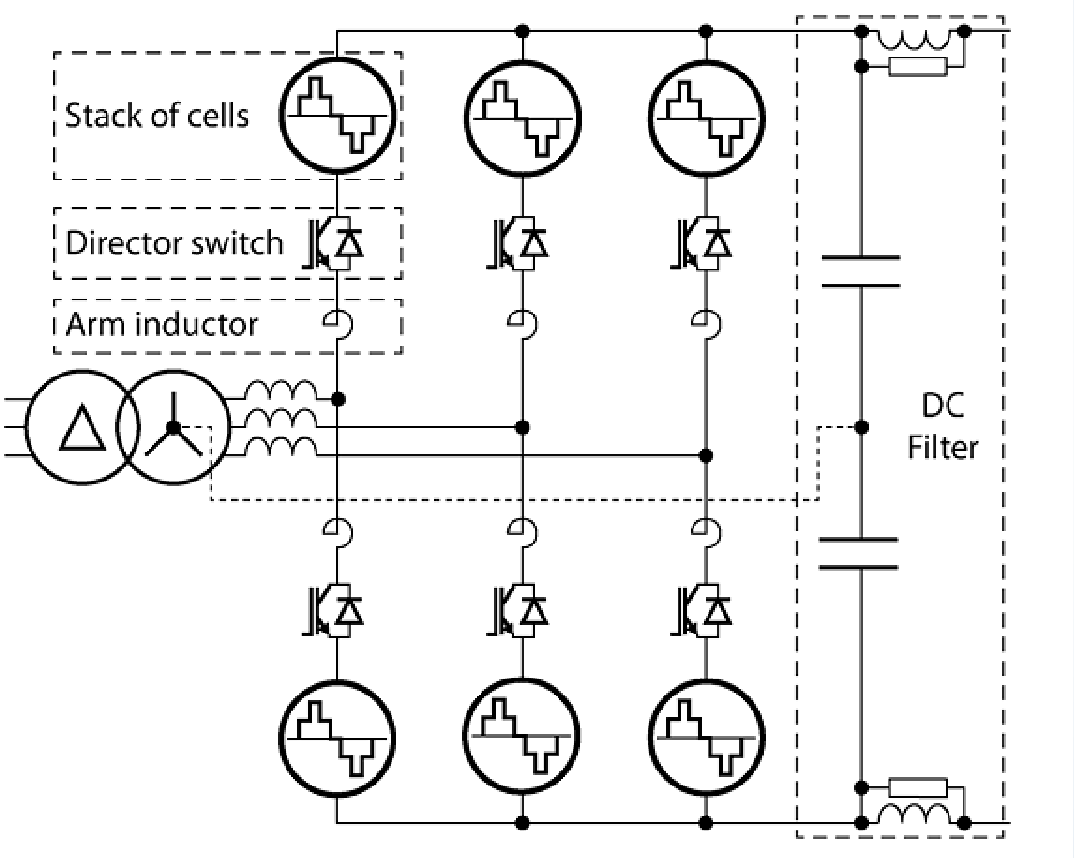
Siemens



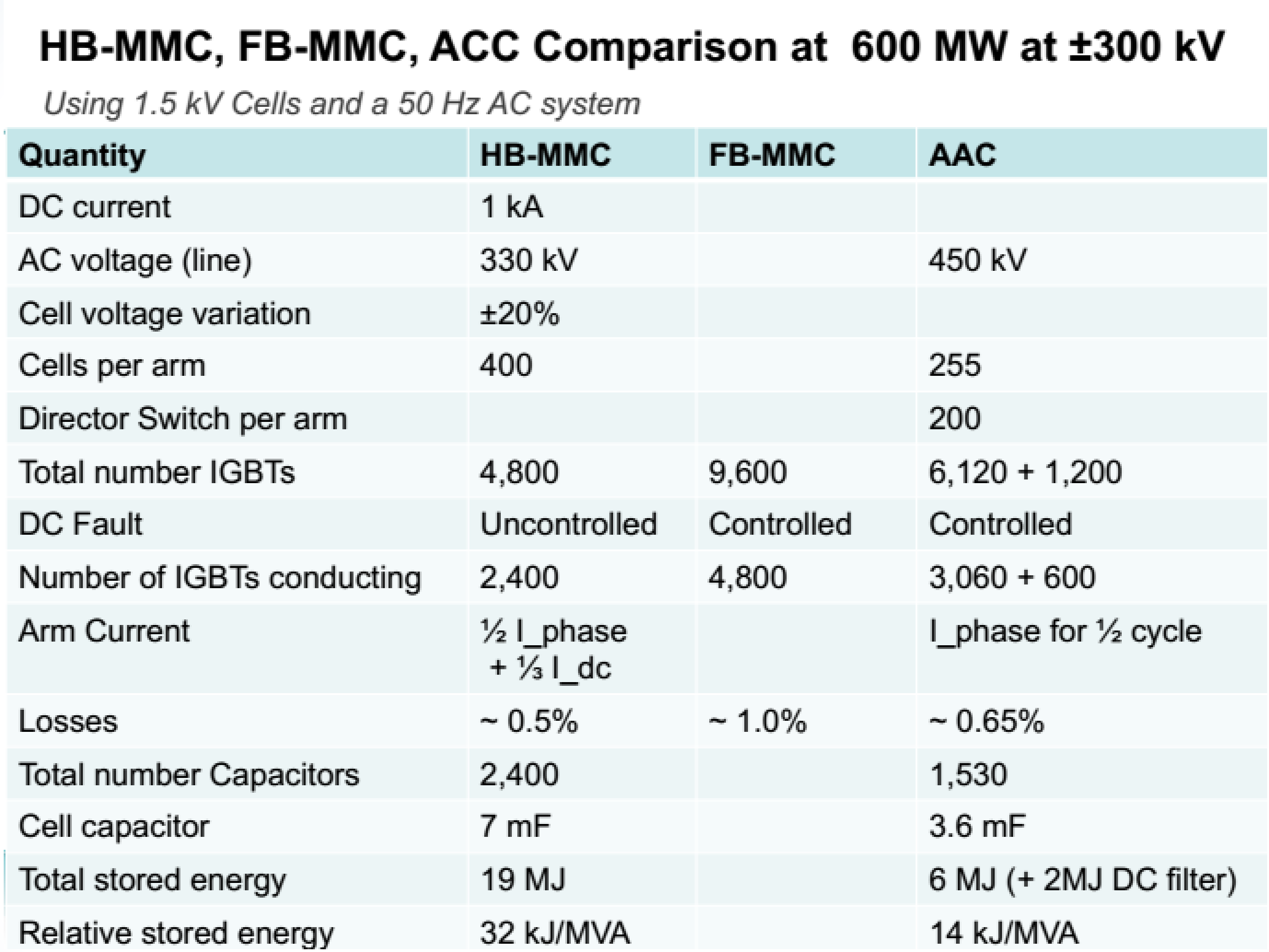
Topologies

Alstom

- DC Fault Tolerant
- Less Switch than F-Bridge
- More Switch than H-Bridge
- Less Smoothness
- Higher Voltage Sub-modules



Topologies



HB-MMC, FB-MMC, ACC Comparison at 600 MW at ±300 kV

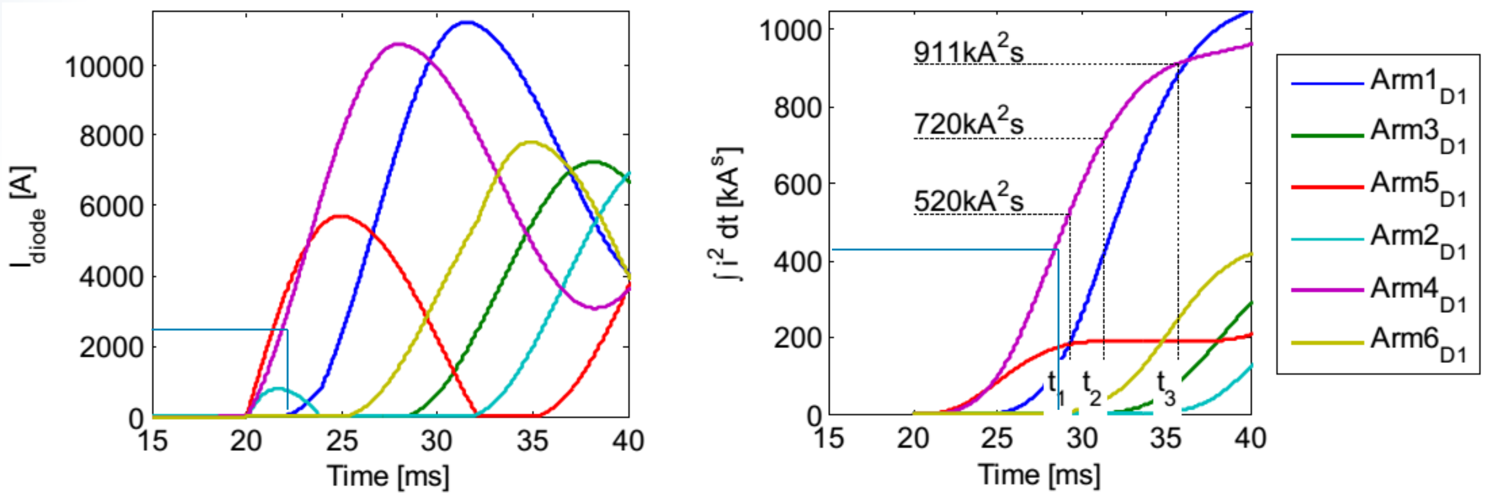
Using 1.5 kV Cells and a 50 Hz AC system

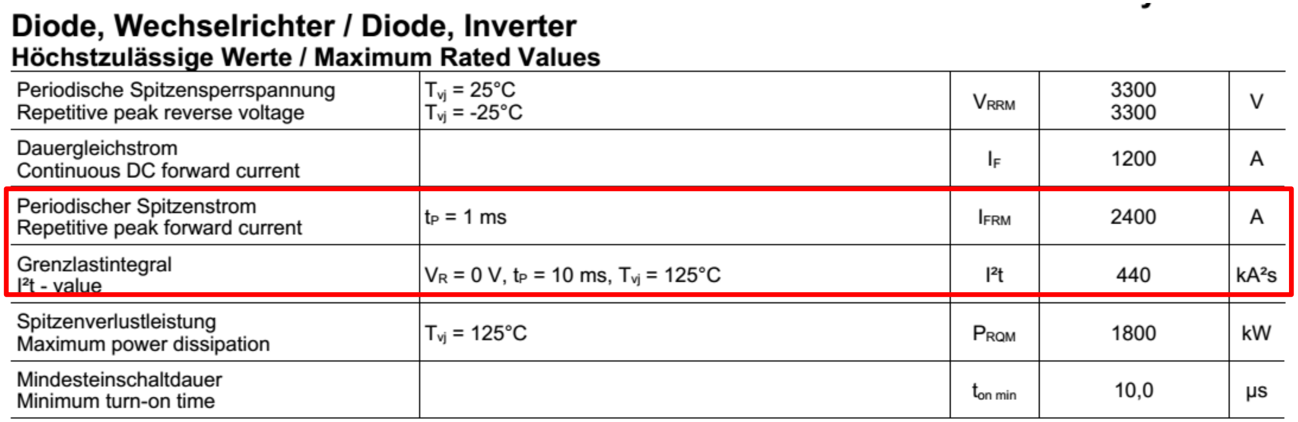
Quantity	HB-MMC	FB-MMC	AAC
DC current	1 kA		
AC voltage (line)	330 kV		450 kV
Cell voltage variation	±20%		
Cells per arm	400		255
Director Switch per arm			200
Total number IGBTs	4,800	9,600	6,120 + 1,200
DC Fault	Uncontrolled	Controlled	Controlled
Number of IGBTs conducting	2,400	4,800	3,060 + 600
Arm Current	½ I_phase + ⅓ I_dc		I_phase for ½ cycle
Losses	~ 0.5%	~ 1.0%	~ 0.65%
Total number Capacitors	2,400		1,530
Cell capacitor	7 mF		3.6 mF
Total stored energy	19 MJ		6 MJ (+ 2MJ DC filter)
Relative stored energy	32 kJ/MVA		14 kJ/MVA

Source: Tim Green’s Presentation at University of Strathclyde, Dec 2014

Topologies

Diode currents in an MMC converter under DC fault conditions





Diode, Wechselrichter / Diode, Inverter

Höchstzulässige Werte / Maximum Rated Values

Periodische Spitzensperrspannung Repetitive peak reverse voltage	T_{vj} = 25°C T_{vj} = -25°C	V_{RRM}	3300 3300	V
Dauergleichstrom Continuous DC forward current		I_F	1200	A
Periodischer Spitzenstrom Repetitive peak forward current	t_P = 1 ms	I_{FRM}	2400	A
Grenzlastintegral I²t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C	I²t	440	kA²s
Spitzenverlustleistung Maximum power dissipation	T_{vj} = 125°C	P_{RQM}	1800	kW
Mindesteinschaltdauer Minimum turn-on time		$t_{on\ min}$	10,0	µs

Source of Figures: Stephen Finney’s Presentation at University of Strathclyde, Dec 2014

Which Topology?

Each One Has Its Pros and Cons

Fault Tolerant Topologies:

- Can Reduce the Need for DC Circuit Breaker
- Have Higher Power Losses
- What about the Selectivity?

Half- Bridge based Topologies:

- Good Efficiency
- Defenceless Against the DC side Faults
- Requires Fast DC Fault Current Breaking

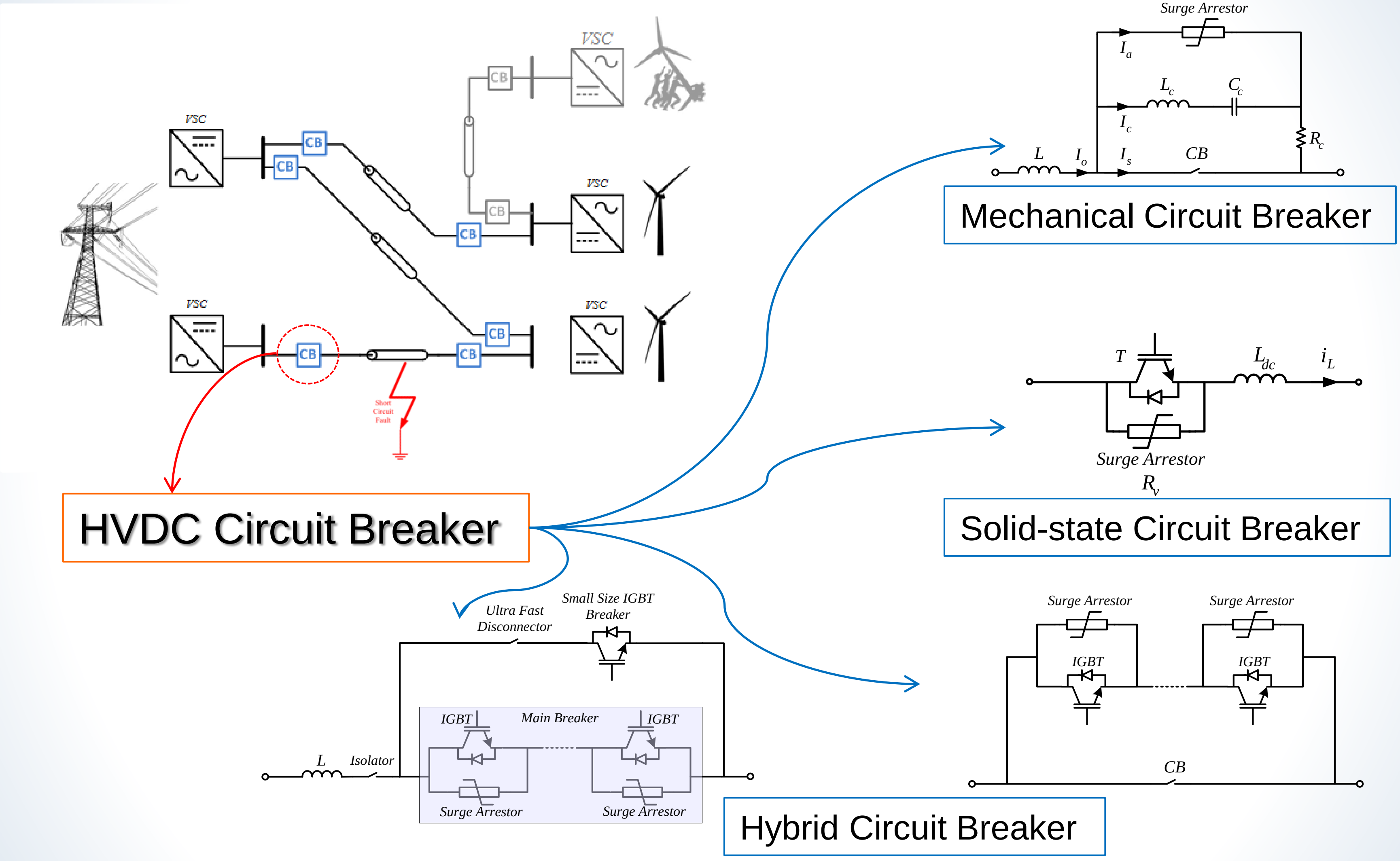
Remarks on DC Grid Protections

Fault causes rapidly changing currents in all lines
Selectivity: Only the affected element must be switched
IGBTs cannot withstand high overloads
Diodes are More Vulnerable
Fast enough (DC: no inductance XL to limit the current)
Only in case of DC fault and not during load change or AC fault

Fault location (branch) detection within a few milliseconds
Too fast for communication between measurement devices
Independent detection systems
Opening at both sides of the faulted line
No opening of other branches?
Backup in case this fails
New superfast DC breakers are needed (≈ 5 ms)

Source: Dirk Van Hertem, Lecture at Strathclyd University, Glasgow, Scotland, Dec 2014

HVDC Circuit Breaker



HVDC Circuit Breaker

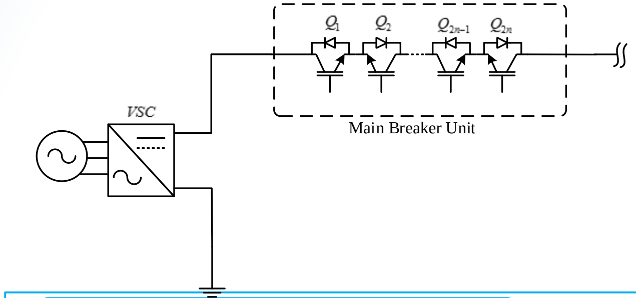
Mechanical Circuit Breaker

Solid-state Circuit Breaker

Hybrid Circuit Breaker

Fast DC Circuit Breakers

Solid-state Circuit Breaker



Interruption Time

- Ultra Fast

Maximum Ratings

- 800kV, 5kA expected

Conduction Losses

- High, up to 30% of Related VSC

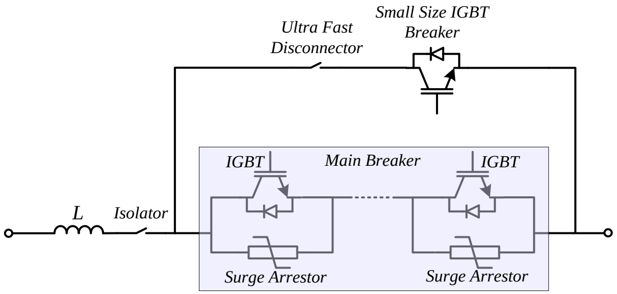
Energy Absorption

- Surge Arrestors

Surge Voltage

- Very High

Hybrid Circuit Breaker



Interruption Time

- Fast

Maximum Ratings

- 320kV, 16kA Expected

Conduction Losses

- Low, up to 1% of Related VSC

Energy Absorption

- Surge Arrestors

Surge Voltage

- Very High

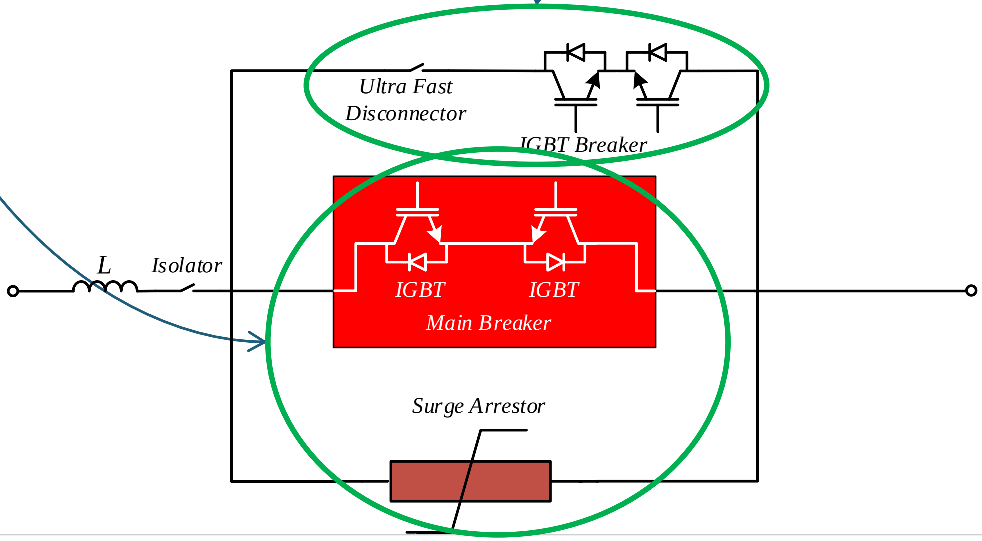
Fast DC Circuit Breakers

Hybrid Circuit Breaker

Solid-state Circuit Breaker + Metal Contacts and Semiconductors

Main interrupter in fault condition

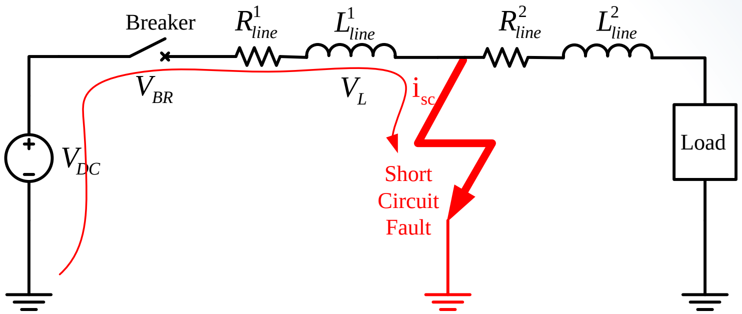
Conducting the current in normal operation

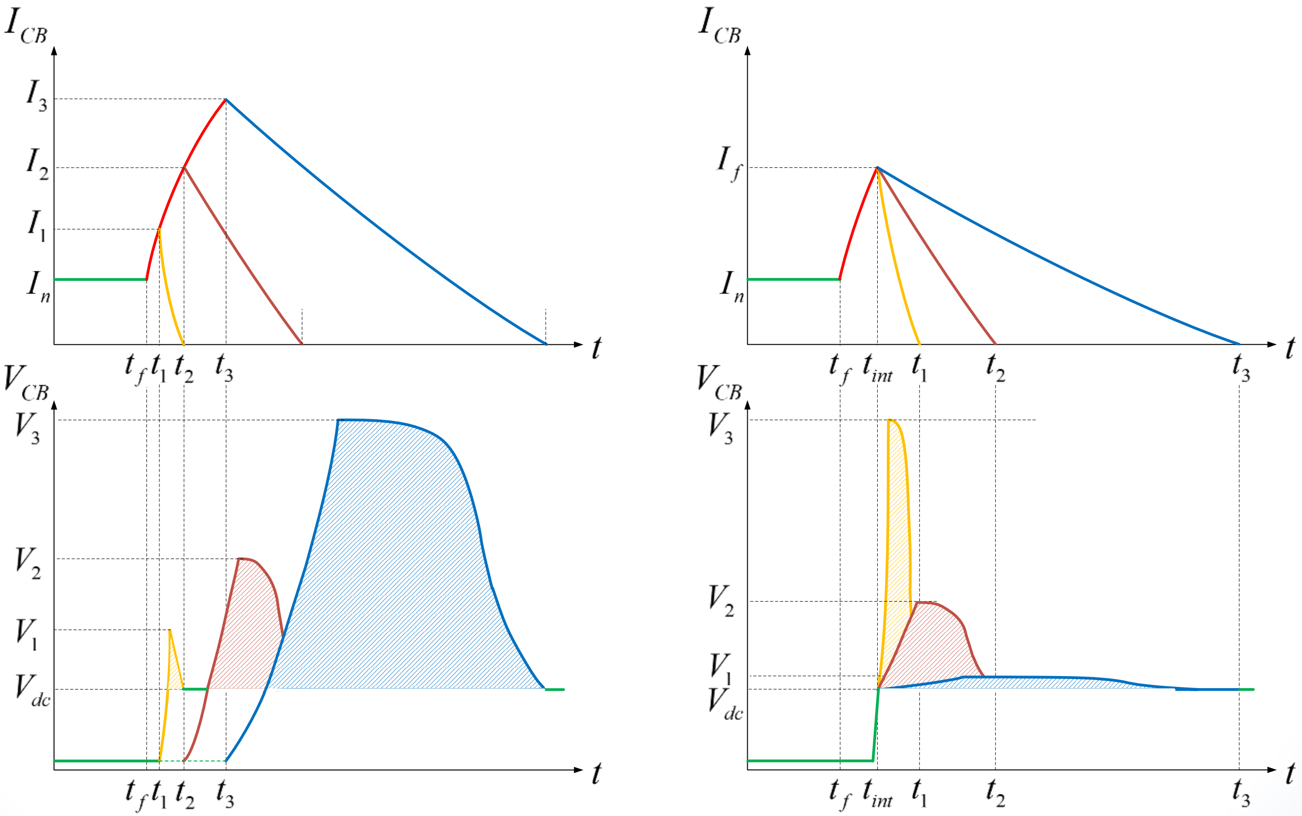


Fast DC Circuit Breakers

$$\boxed{I_{sc} = I_n + \frac{di_f}{dt}\cdot t_{delay}}$$

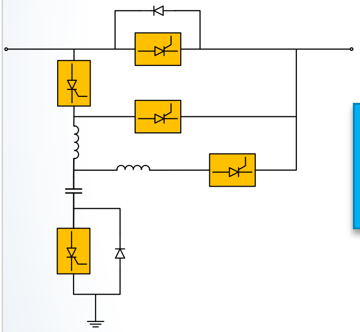
$$\boxed{V_{CB} = V_{DC} - R_{line}.i_{sc} - L_{line}\cdot\frac{di_{sc}}{dt}}$$

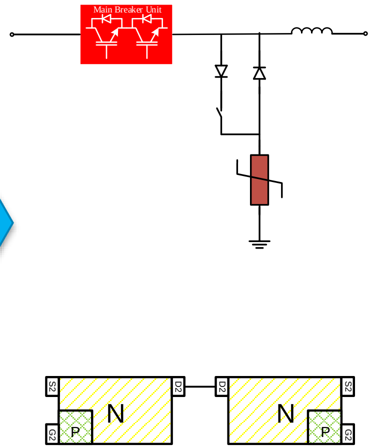


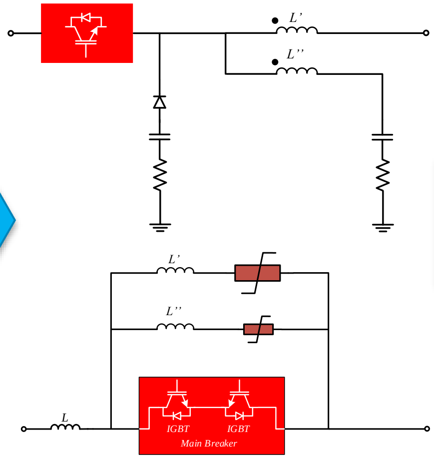


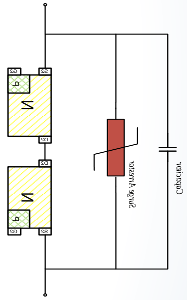
Fast DC Circuit Breakers

Two Main Solid-state DC Circuit Breaker Topologies









2010
Thyristor based

2013
1-Diode+Rv based
2-SiC-BGSIT based

2014
1-Coupled Inductors based
2-Seperated Rv based

2015
SiC based

General Requirements

Quick Interruption Action

- High rate of rise of fault current
- Save converters
- Protec. algorithms
- Footprint

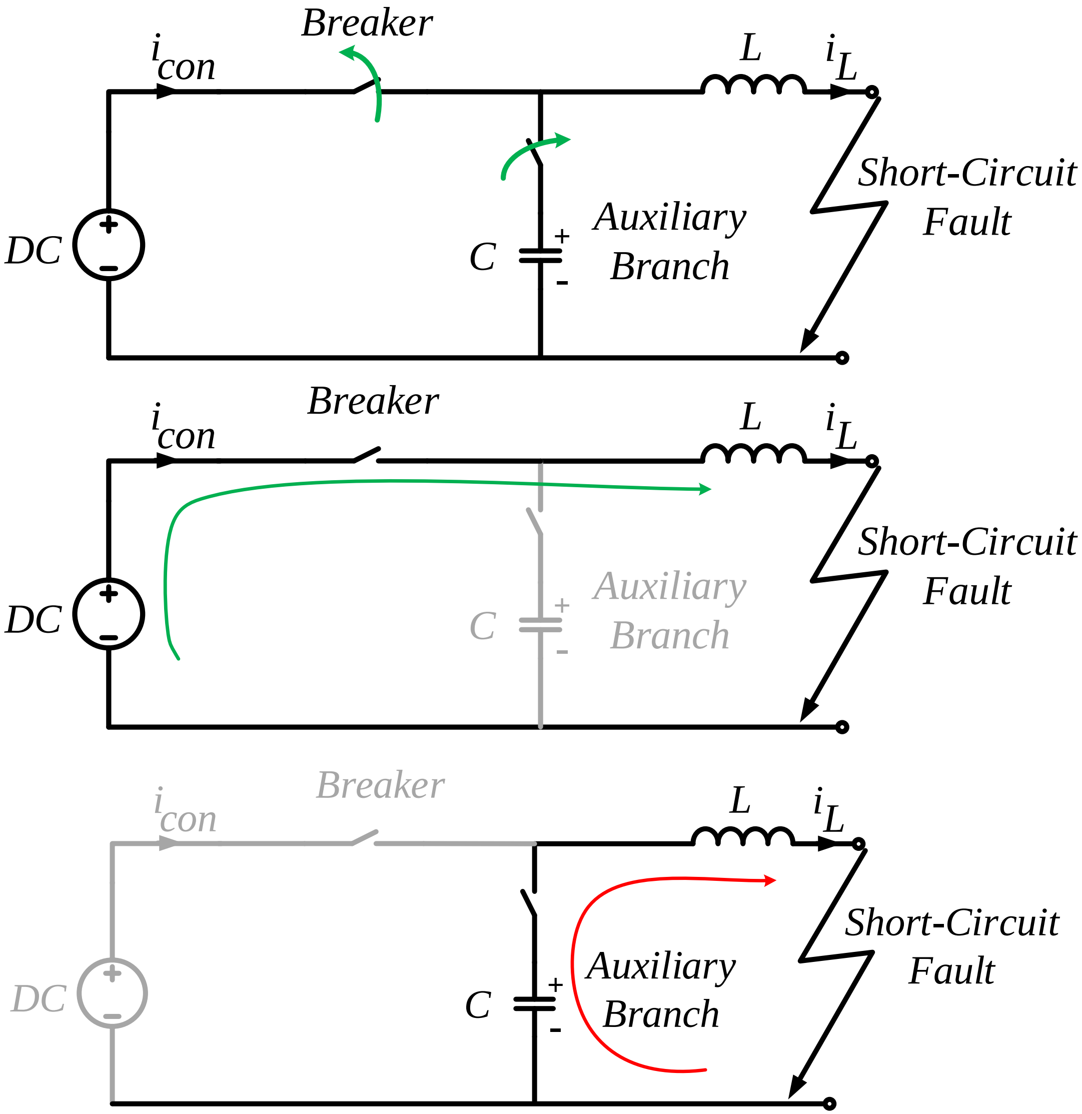
Stored Energy Dissipation

- Surge arrestor
- Limitations as energy absorbers
- Reducing the Reliability of the Device

Surge Voltage Issue

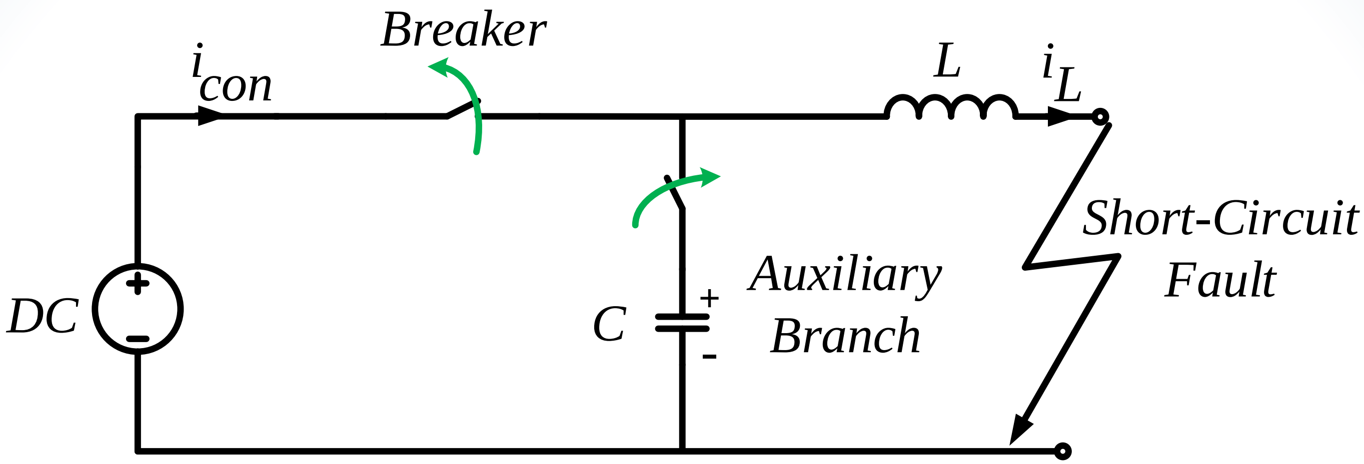
- Surge arrestor
- High overvoltage
- Insulation problem
- Increase the cost of devices

Proposed Method



Pending Patent, No. 108775, 2015, Ataollah Mokhberdoran, Adriano Carvalho, Nuno Silva, Hélder Leite, António Carrapatoso

Proposed Method



Employs a pre-charged capacitor

To feed the fault current during and after main breaker unit interruption

Prevent the sudden reduction of voltage of beginning of the line

Change the final equivalent circuit to a RLC circuit

No surge Voltage

Natural response of the RLC circuit

Ultra-fast action

The converter current is interrupted very quickly (in the range of few hundred micro seconds)

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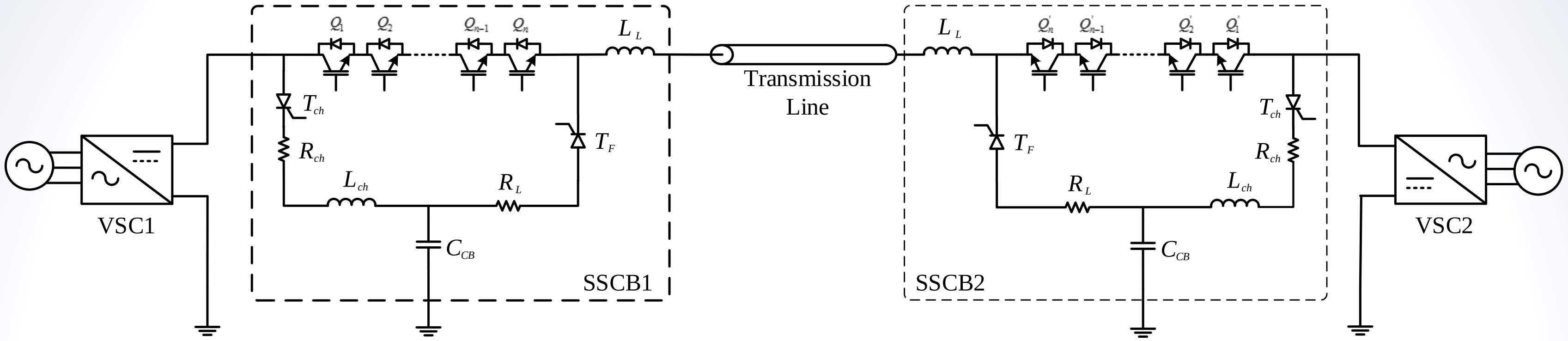
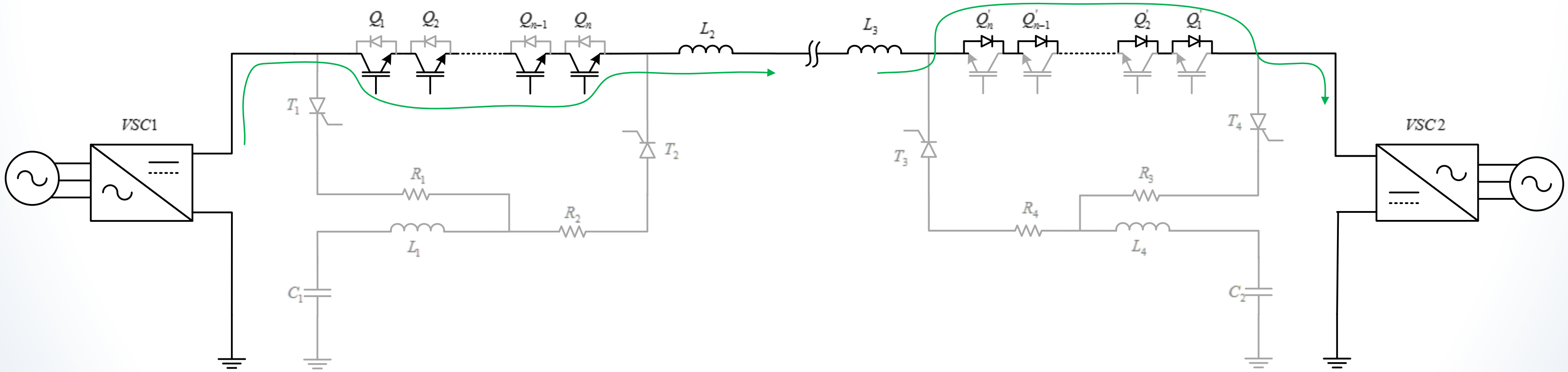
SSCB in A System





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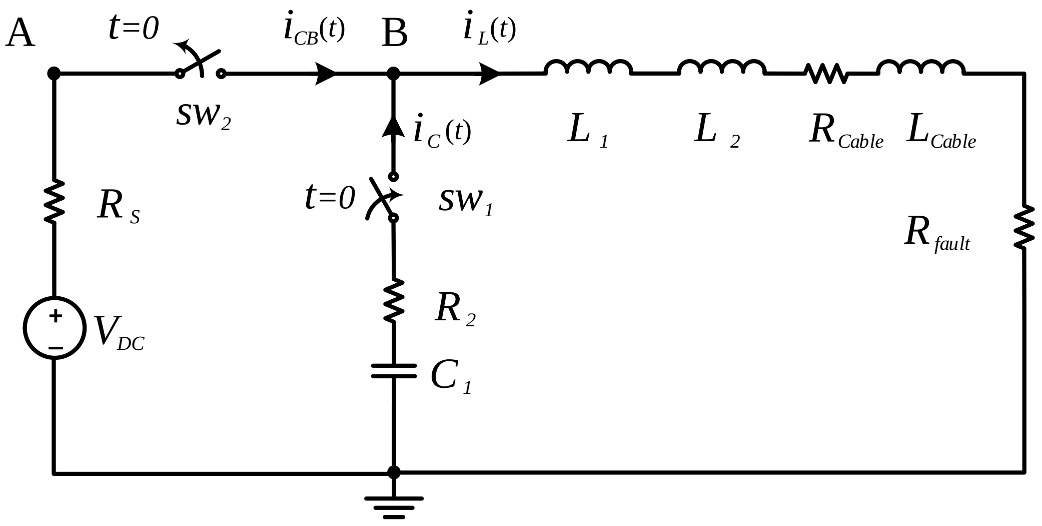
Aggregated Model



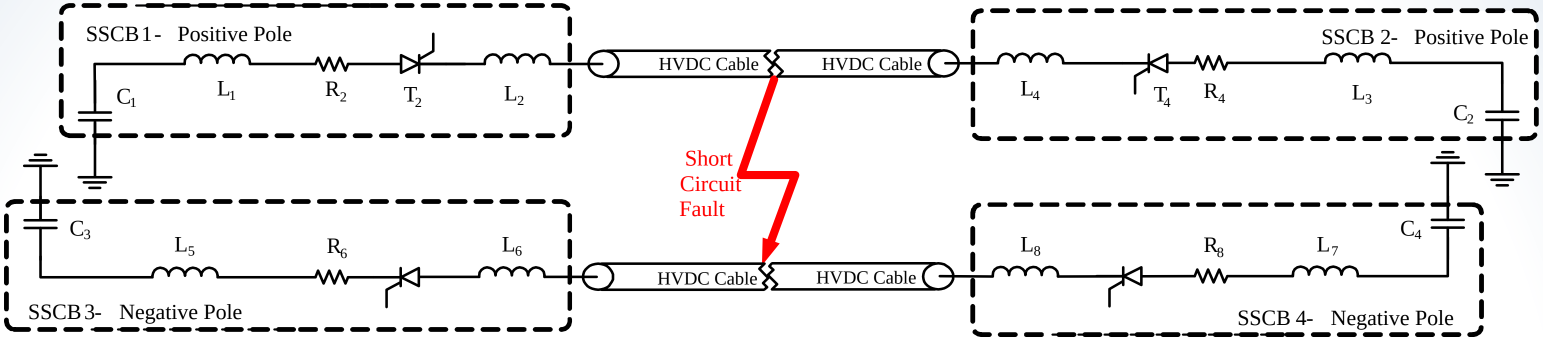
$$\frac{d^2 i(t)}{dt^2} + \frac{\left(R_2 + R_{fault} + R_{cable}\right)}{\left(L_1 + L_2 + L_{cable}\right)}\frac{di(t)}{dt} + \frac{1}{\left(L_1 + L_2 + L_{cable}\right).C_1} i(t) = 0$$

$$\xi = \frac{\left(R_2 + R_{fault} + R_{cable}\right)}{2}\sqrt{\frac{C_1}{\left(L_1 + L_2 + L_{cable}\right)}}$$

$$R_2 = \frac{V_{C_1}}{k.I_{\max}}$$

$$C_1 > \frac{4 \times \left(L_1 + L_2 + L_{cable}\right)}{\left(R_2\right)^2}$$

Aggregated Model



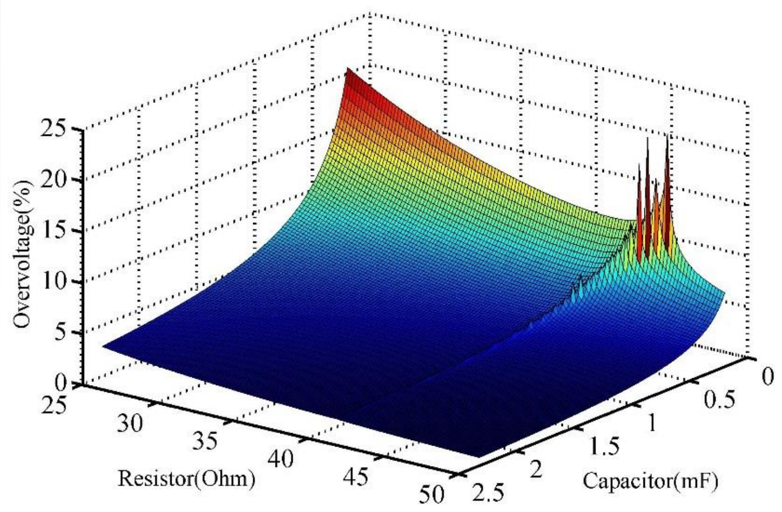
$$\xi = \frac{\left(2\times R_2 + R_{fault} + 2\times R_{cable}\right)}{2}\sqrt{\frac{\left(C_1/2\right)}{2\times\left(L_1 + L_2 + L_{cable}\right)}}$$

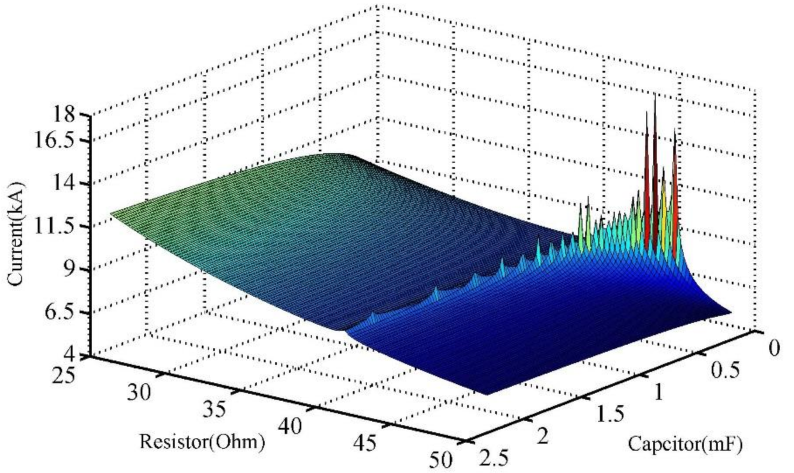
$$\xi \simeq \frac{\left(R_2 + R_{fault} + R_{cable}\right)}{2}\sqrt{\frac{C_1}{\left(L_1 + L_2 + L_{cable}\right)}}$$

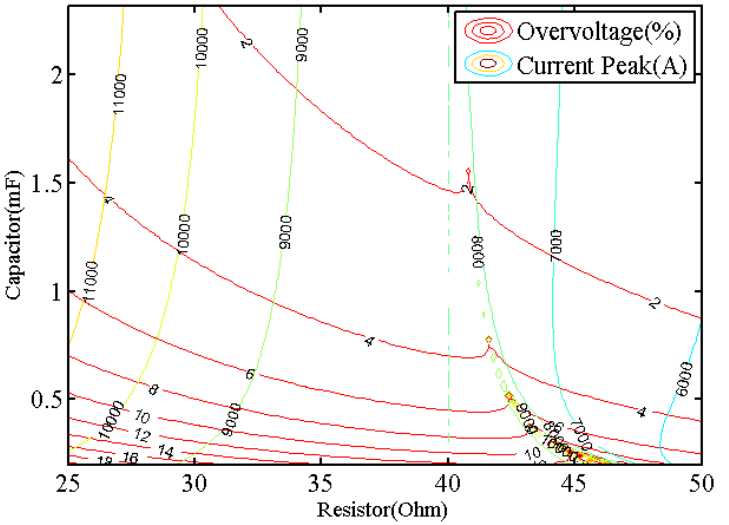
$$\boxed{R_2 = \frac{V_{C_1}}{k.I_{\max}}}$$

$$\boxed{C_1 > \frac{4\times\left(L_1 + L_2 + L_{cable}\right)}{\left(R_2\right)^2}}$$

Aggregated Model







SSCB in A System

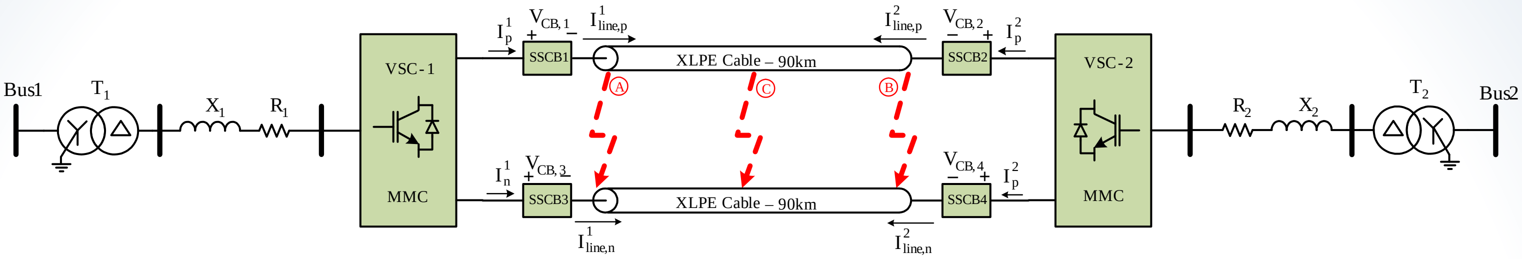


Table I: Assumed system parameters

MMC Power	1000MVA	Cable Length	90km	Transformer	Y/D
Nominal Voltage	±320kV	Smoothing Reactor	15mH	AC source	230kV
Configuration	Sym. monopole	Fault Impedance	0.1Ω	MMC Type	Half-bridge

Table II: Designed SSCB parameters

I_{th}	3kA	R_1	3kΩ	L_1	50µH
C_1	350µF	R_2	30Ω	L_2	10mH

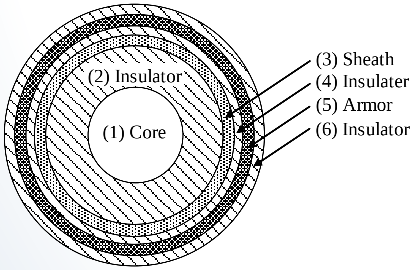
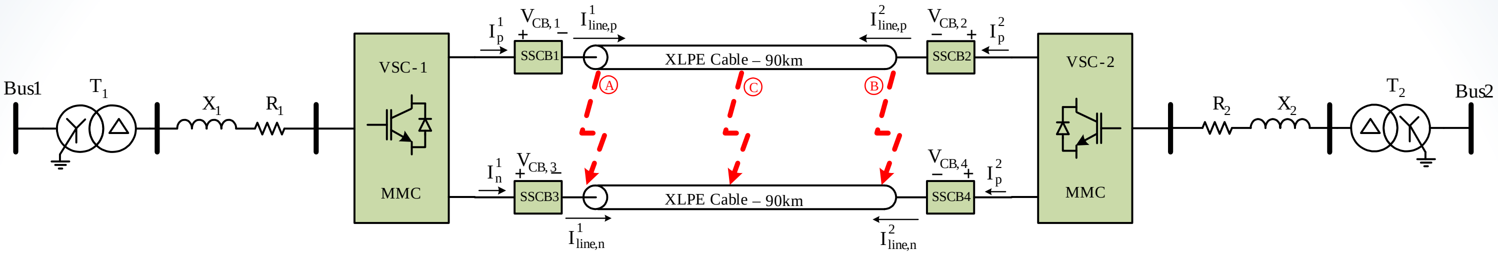
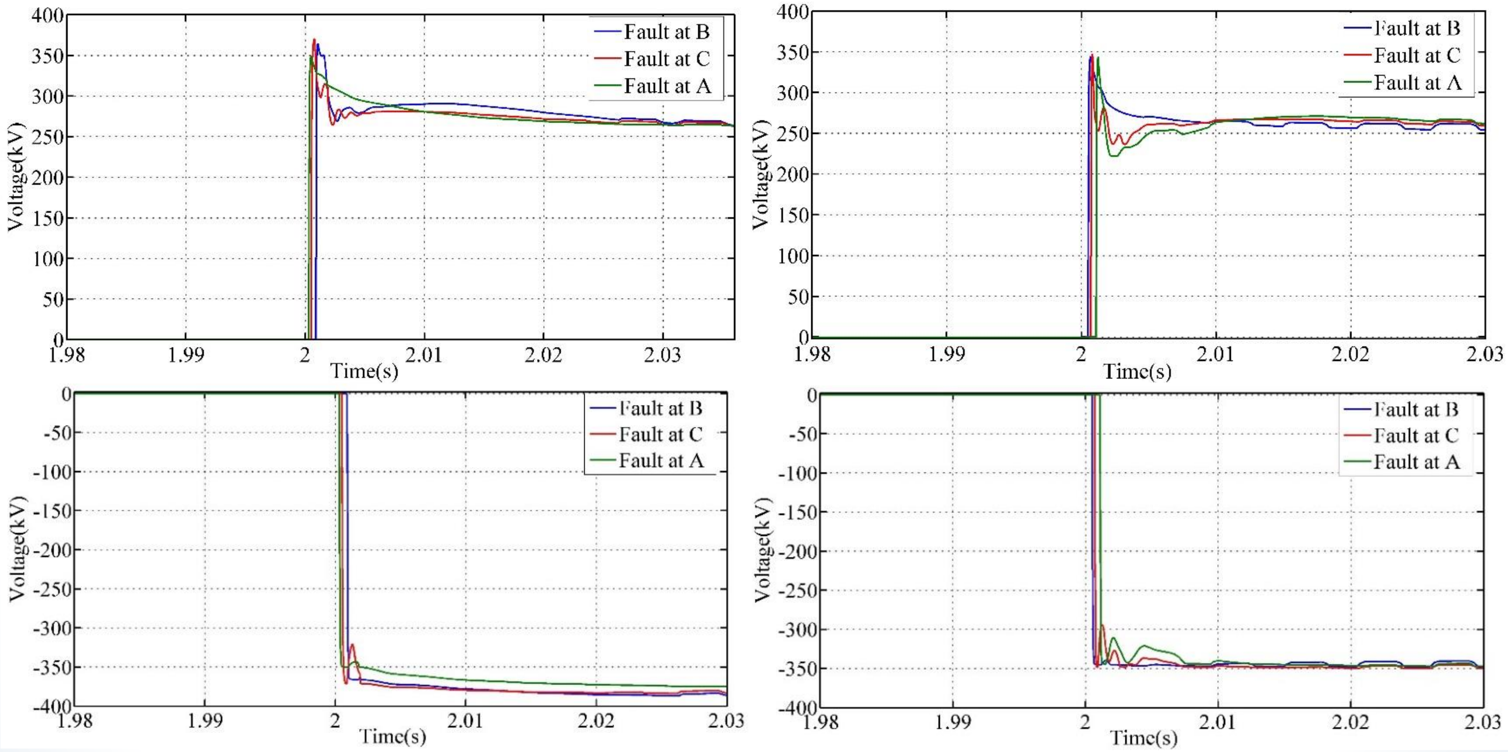


TABLE III
DC CABLE DATA

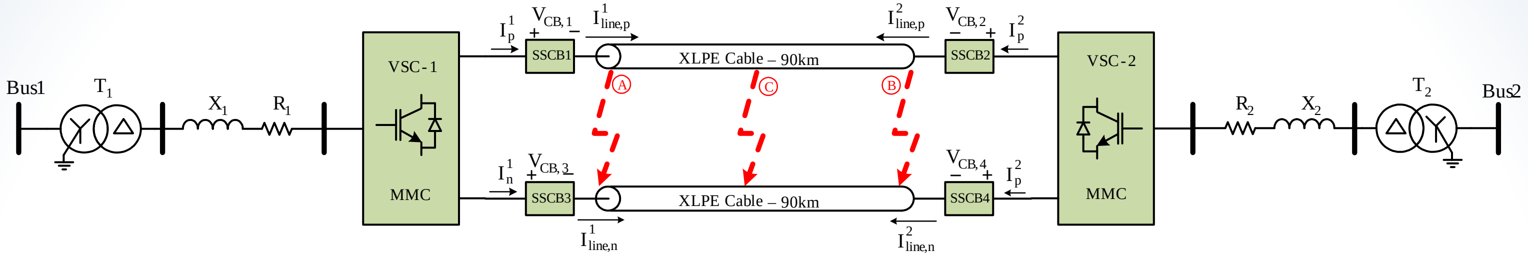
Layer	Radius (mm)	Resistivity (Ωm)	Rel. permeability	Rel. permittivity
(1) Core	25.2	$1.72*10^{-8}$	1	1
(2) Insulator	40.2	-	1	2.3
(3) Sheath	43.0	$2.20*10^{-7}$	1	1
(4) Insulator	48.0	-	1	2.3
(5) Armor	53.0	$1.80*10^{-7}$	10	1
(6) Insulator	57.0	-	1	2.1

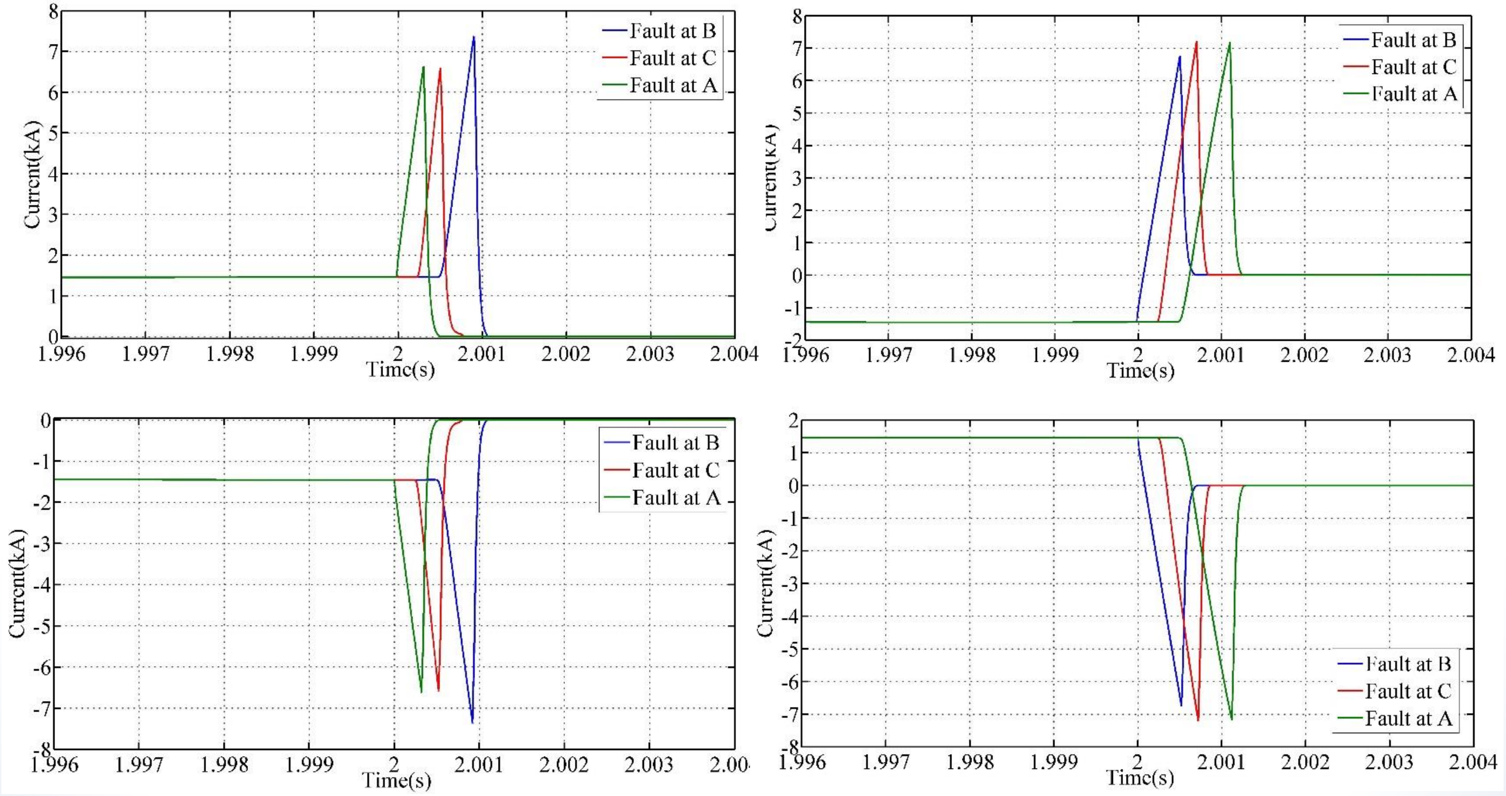
Point to Point MMC-HVDC



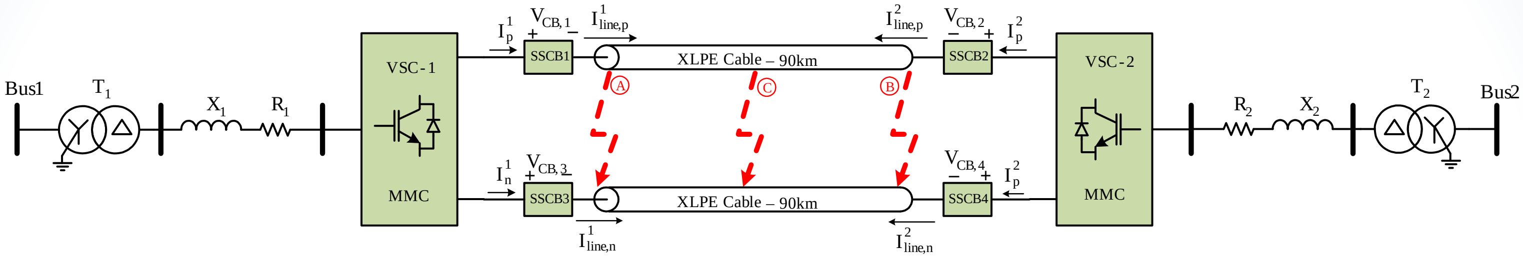


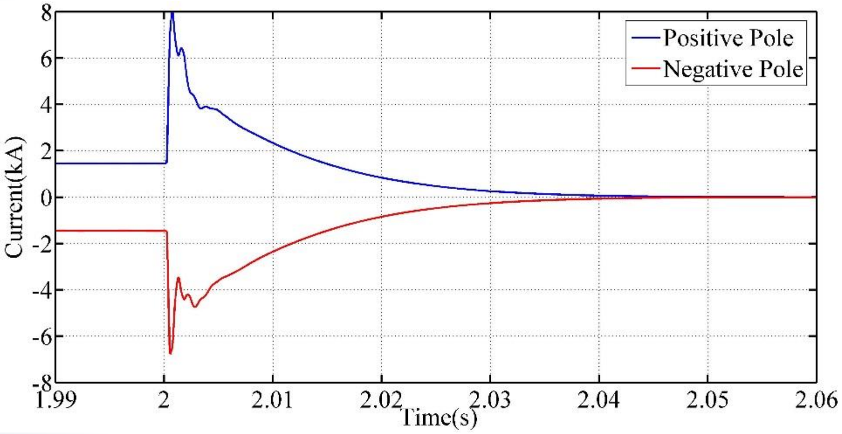
Point to Point MMC-HVDC

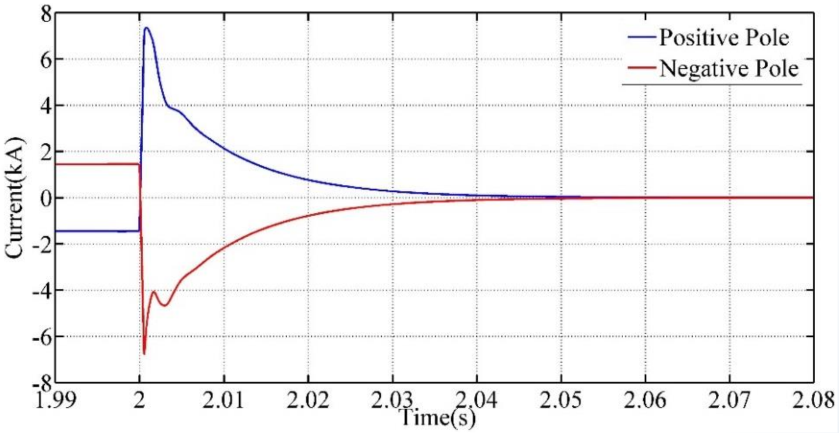




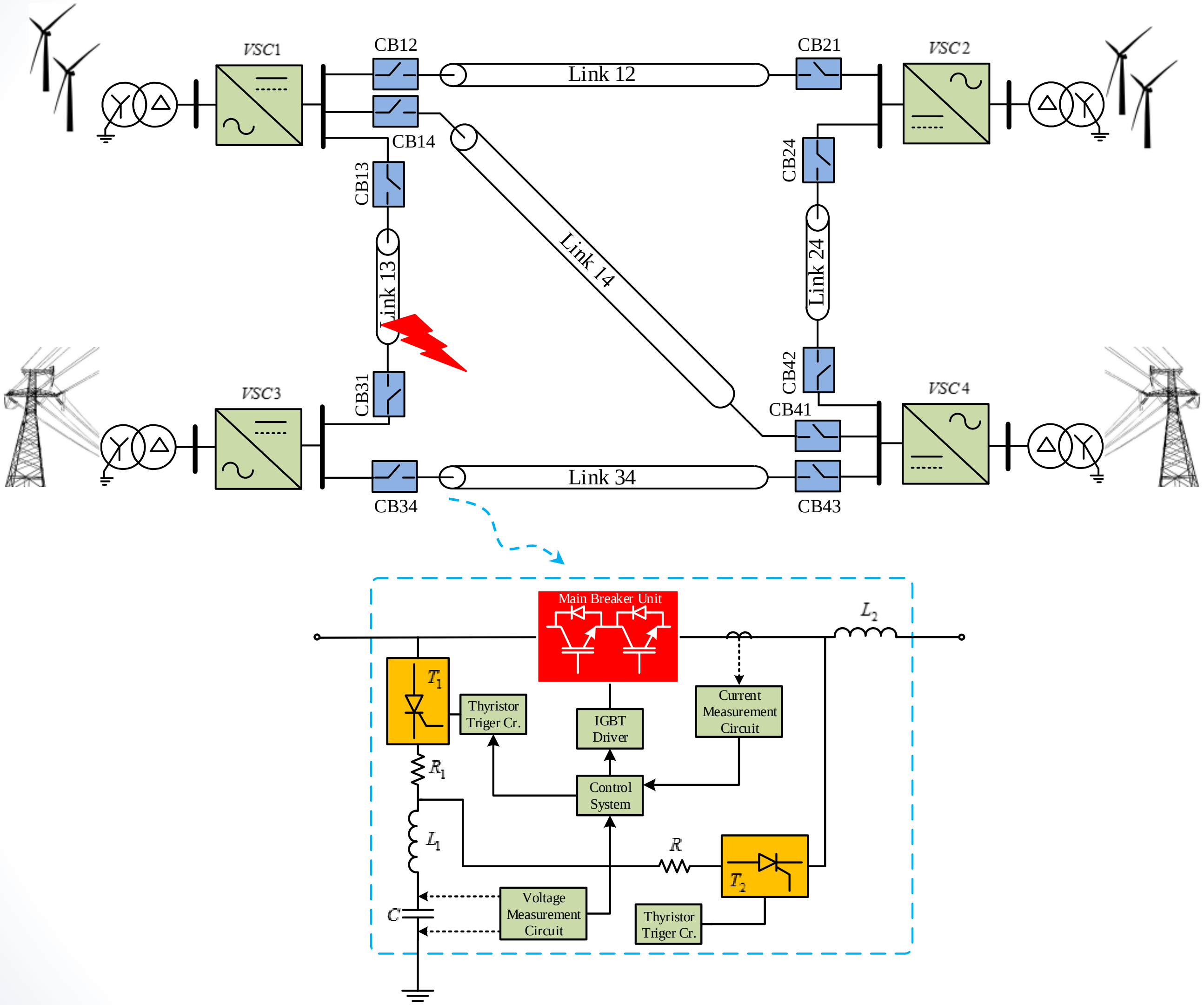
Point to point MMC-HVDC





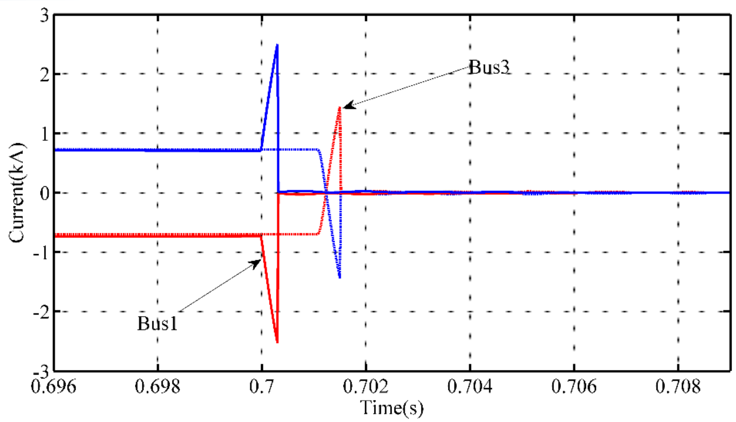


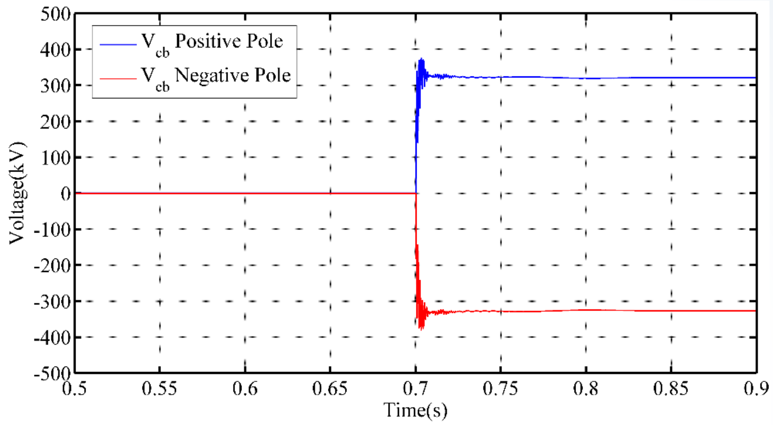
Multi-Terminal Model



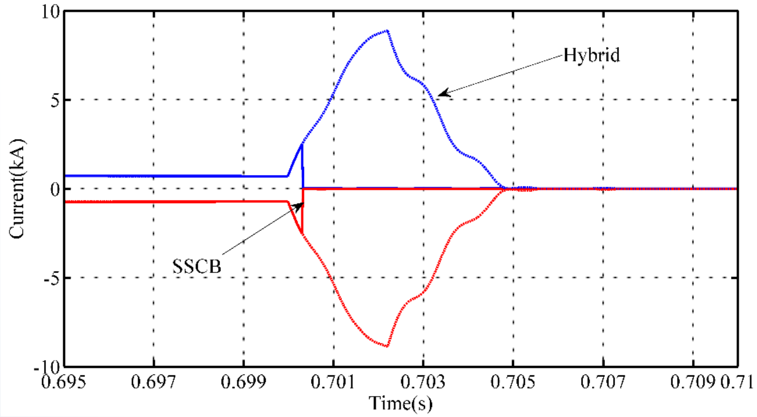
Multi-Terminal Model

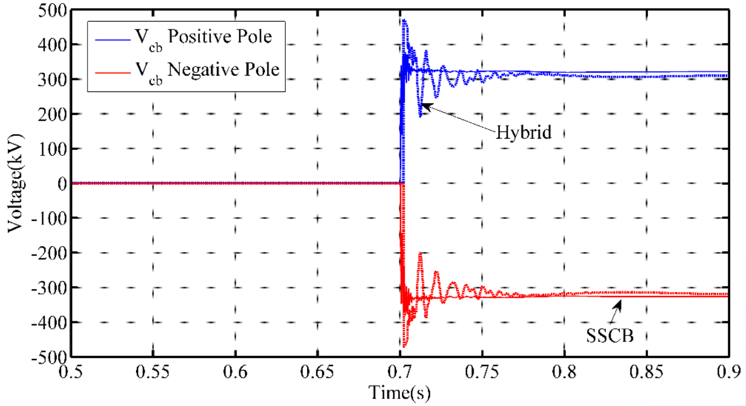
Fault Close to Bus1





SSCBs are installed





Comparison

Developed Topology of SSCB

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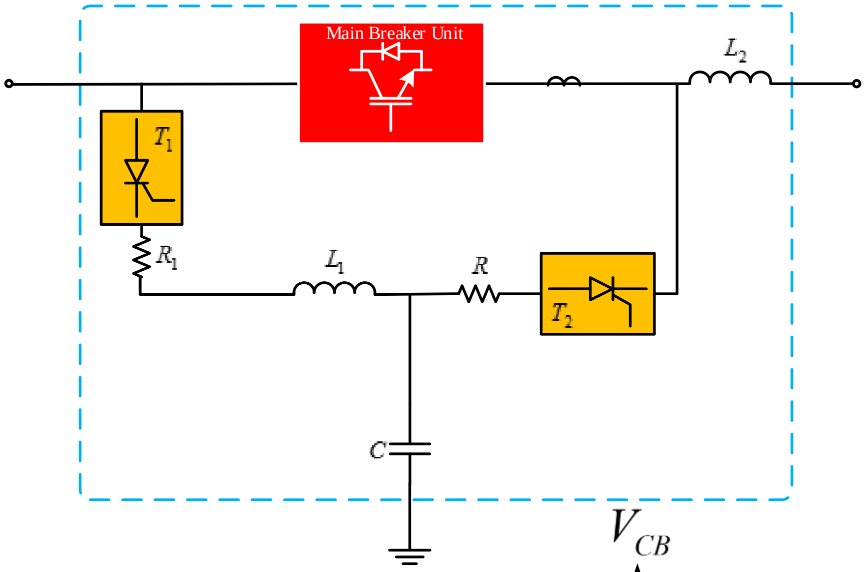
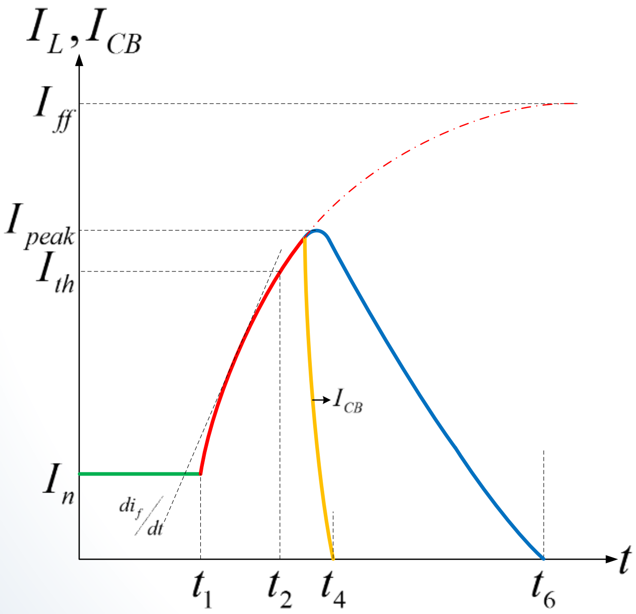
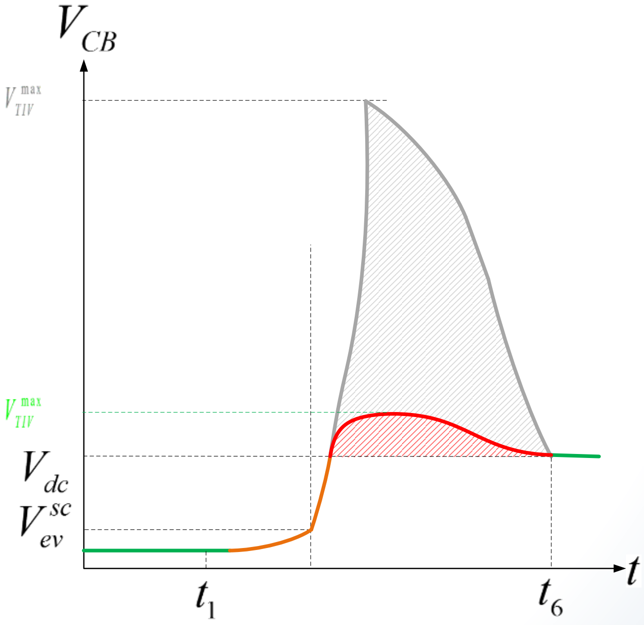
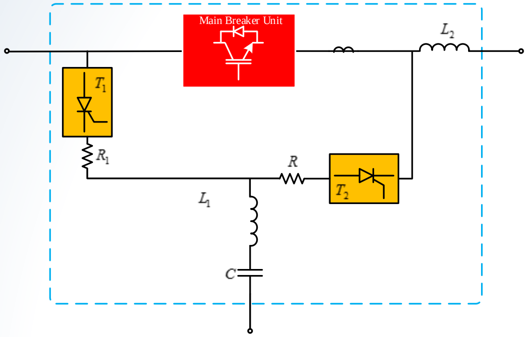
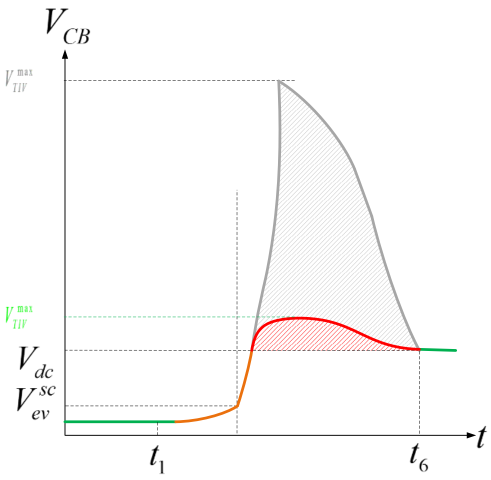


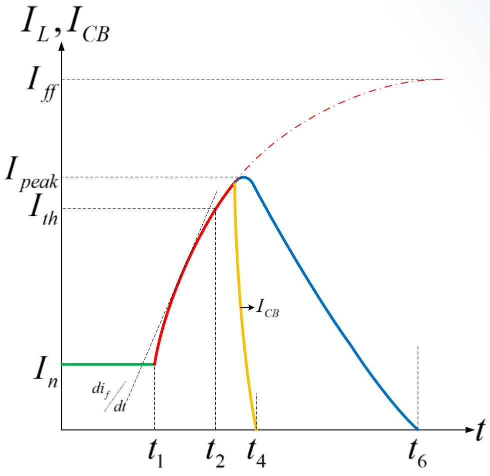


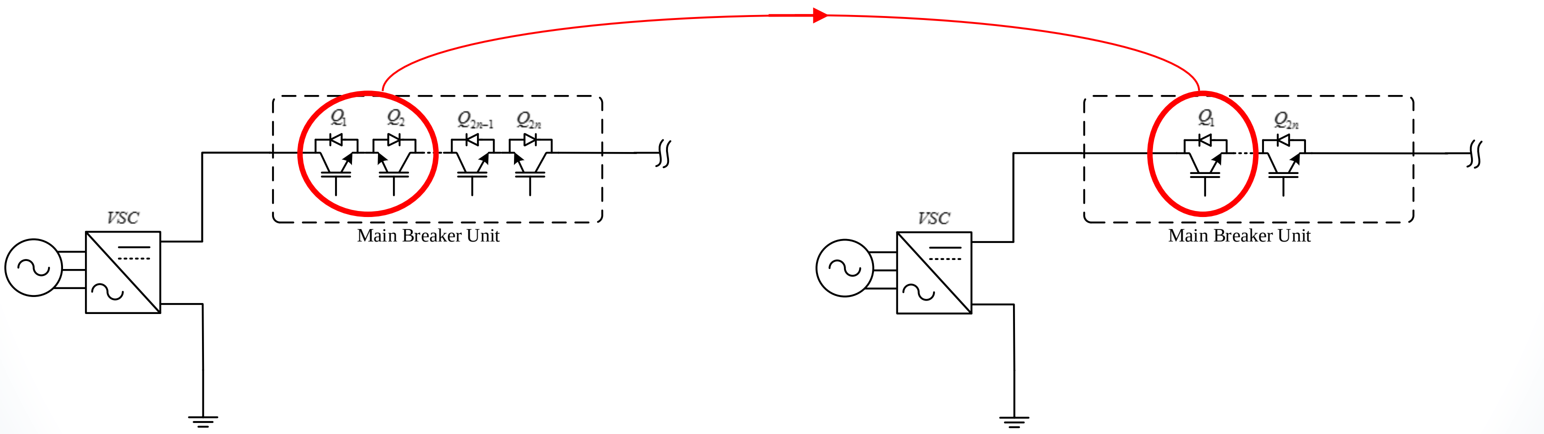


Developed Topology of SSCB









$$P_{loss} = N_{sw} \times V_{sat} \times I_{CB}$$

Summary

Fault Tolerant Converters can Reduce the Need for DCCB but not Eliminate

Pre-Block Current Stress Must be Considered in Sizing of IGBTs

Pre-Bypass Stress on Anti-Parallel Diodes, Specially Surge Current

Impact of VSC Control during the DC Fault should be Studied

- New DC Fault Current Breaking Concept Proposed
- Employs Common Components
- Shows Improved Characteristics

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Thank you for your attention

Questions?


Photo by: Ataollah Mokhberdoran